
Errata: Answers to Exercises/Problems
An Introduction To Mixed-Signal IC Test and
Measurement, Burns/Roberts, Oxford University
Press.

Updated March 27, 2003

Chapter 1

Solution set at back of book had an extra answer that did not belong there. Problem number realignment is shown below.

- 1.8 Short between metal traces (i.e. blocked etch). Bonus answer: Can also cause a gap in the trace, if using a negative process.
- 1.9 A clean room eliminates particles in the air, thus reducing the particulate defects such as those in Figure 1-8.
- 1.10 Wafer probe testing, bond wire attachment into lead frames, plastic encapsulation (injection molding), lead trimming, final testing.
- 1.11 Two devices do not represent a good statistical sample from which to draw conclusions. Need data from hundreds or thousands of devices.
- 1.12 Mainframe, test head, user computer, system computer, DIB
- 1.13 Provides a temporary electrical interface between the ATE tester and the DUT. Also provides DUT-specific circuits such as load circuits and buffer amplifiers.
- 1.14 Wafer prober
- 1.15 Requires proactive test engineering, better communications between test and design engineering, coordinated engineering effort.
- 1.16 Allows design engineers and test engineers to agree upon an appropriate set of tests. Also serves as test program documentation.
- 1.17 Time to market, accuracy/repeatability/correlation, electromechanical fixturing, economics of production testing (test economics)

- 1.18 We have to test a total of 5,555,555 devices to get 5 million good ones since we have a 90% yield (yield = ratio of good devices to total devices tested). For the good devices, the time saved is 1.5 seconds times 5 million devices, or 7.5 million seconds of reduced test time per year. Multiplying this by 3 cents per second, we get a total savings of \$225,000 per year in reduced testing costs for the good devices. Multiplying the 0.5 second test time reduction for the bad devices by 555,555 devices per year, we see an additional savings of 3 cents per second times 0.5 seconds times 555,555 devices, or \$8333 per year. Thus the total test cost savings is \$233,333 per year.
- 1.19 The after-tax profit margin is 12.8% (20% times 100%-36%). Therefore, we would have to ship $\$233,333/12.8\% = 1.823$ million dollars worth of product to equal the extra profit offered by the reduced test time. Thus, we have to ship approximately one million extra devices to get the same incremental profit as we get from the 1.5 second test time reduction for this device. Obviously, reducing test time can have as high an impact on profits than selling and shipping millions of extra devices!

Chapter 2

Chapter 3

Exercises:

- E3.5 Problem definition error: Consider the offset voltage over a -5 V to $+5\text{ V}$ range. $+0.477\text{ V}$ (input offset); $+5\text{ V}$ (output offset).
- E3.6 83.3%

Problems:

- 3.9 Two possible input-referred offset voltages: $+0.48\text{ V}$ and -10.48 V ; 5 V output offset.
- 3.15 8 V , 11.5 V , 3.5 V/V , 10.88 dB . (Question clarification: What is the corresponding gain of this amplifier in V/V over a 1 V swing centered about 2.5 V ?)
- 3.16 2.85 V , 8.65 V , 2.9 V/V , 9.25 dB . (Question clarification: What is the corresponding gain of this amplifier in V/V over a 2 V swing centered about 2 V ?)
- 3.18 1.347 mV
- 3.27 1st iteration: point1 = $(-1\text{ V}, -7.5\text{ V})$, point2 = $(+1\text{ V}, 4.5\text{ V})$, estimated zero crossing at 250.0 mV ; 2nd iteration: point1 = $(+1\text{ V}, 4.5\text{ V})$, point2 = $(250.0\text{ mV}, -$

468.7 mV), estimated zero crossing at 320.7 mV; 3rd iteration: point1 = (250.0 mV, -468.7 mV), point2 = (320.7 mV, -24.0 mV), estimated zero crossing at 324.5 mV; 4th iteration: point1 = (320.7 mV, -24.0 mV), point2 = (324.6 mV, -0.14 mV), estimated zero crossing at 324.5 mV; 5th iteration: point1 = (324.6 mV, -0.14 mV), point2 = (324.6 mV, -42.8 nV), estimated zero crossing at 324.5 mV; – converged with 5 iterations. Input offset voltage is approximately –324.5 mV. A binary search would have taken 10 iterations to achieve a 1 mV convergence.

Chapter 4

Exercises:

E4.6

$$v_{\text{calibrated}} = \frac{-G_1 + \sqrt{G_1^2 + 4G_2(v_{\text{measured}} - \text{offset})}}{2G_2} \quad \text{or} \quad v_{\text{calibrated}} = \frac{-G_1 - \sqrt{G_1^2 + 4G_2(v_{\text{measured}} - \text{offset})}}{2G_2}$$

E4.9 Missing question information (answer in book is correct): *A voltmeter is specified to have an accuracy of ±1% of programmed range. If a 0.5 V DC signal is measured on a ±1 V range, what is the minimum and maximum DC levels that might have been present at the meter's input during this measurement?*

Problems:

Chapter 5

Solution set at back of book had an extra answer that did not belong there. Problem number realignment is shown below.

- 5.5 Kelvin connections compensate for the IR voltage drops in the high force line and current return line of a DC source.
- 5.6 A local relay can provide a low noise ground to the DUT inputs. (Alternate answer, can provide local connections to load circuits, buffer amplifiers, and other sensitive DIB circuits).
- 5.7 Flyback diodes prevent inductive kickback from the relay coil from damaging the drive circuitry.
- 5.8 A digital pattern generates digital 1/0 waveforms and high/low comparisons. A digital signal contains waveform information such as samples of a sine wave.

- 5.9 The number of vectors in the frame loop and the frequency of the digital vectors in a sampling frame determine the sampling frequency of the mixed-signal circuit (DAC or ADC, for example).
- 5.10 Source memory stores digital signal samples and supplies them to a mixed-signal circuit such as a DAC.
- 5.11 Capture memory captures and stores digital signal samples from a DUT circuit such as an ADC.
- 5.12 The DAC samples are written at a frequency equal to $6 \text{ MHz} / 600 = 10 \text{ kHz}$. The total time to supply all 256 samples to the DAC is equal to $256 * (1 / 10 \text{ kHz}) = 25.6 \text{ ms}$.
- 5.13 X's are required to place the driver into a HIZ state so that data from the DUT can be read from SDATA. Otherwise the driver would be fighting the output of the SDATA serial interface.
- 5.14 Formatting and timing information is combined with one/zero information to reduce the amount of digital pattern memory required to produce a particular digital waveform. It also reduces the required vector (bit cell) rate for complex patterns – see Figure 5.11. Finally, it gives us better control of edge placement.
- 5.15 The waveforms would be as shown below. The NRZ waveform could be produced using clocked digital logic operating at 2 MHz. The RZ waveform would require clocked digital logic operating at a period of 100 ns, or 10 MHz. If the stop time for the RZ formatted waveform had to be delayed to 901 ns, we would need digital logic operating at a clock rate of 1 GHz.
- 5.16 The CW source and RMS voltmeter are only able to measure a single frequency during each measurement, leading to long test times compared to DSP-based testing. Also, the RMS voltmeter can't distinguish between the DUT's signal and its distortion and noise.
- 5.17 The low-pass filter is used to reconstruct, or smooth, the stepped waveform from the AWG's DAC output.
- 5.18 The PGA sets the measurement range, reducing the effects of the digitizer's ADC quantization error.
- 5.19 Distributed DSP processing reduces test time by splitting the processing task among several processors that perform the mathematical operations in parallel.

Chapter 6

- 6.14 2.0426 Mhz.
- 6.21 62.5 Hz, 125 Hz, 187.5 Hz, 250 Hz, 312.5 Hz, 375 Hz, 437.5 Hz, 550 Hz.

6.23 Problem requires at least six tones to make much sense.

6.26 Spectral bins: 23, 47, 67 and 91 when $N=4096$ and $UTP=91.4$ ms.

Chapter 7

Exercises:

$$E7.7 \quad x[n]=0.6150 \sin[(2\pi/8)n] - 0.2749 \sin[2(2\pi/8)n] - 0.1451 \sin[3(2\pi/8)n] \\ + 0.0649 \sin[4(2\pi/8)n]$$

$$E7.9 \quad x[n]=0.25+(0.5-j0.25)e^{j(2\pi/10)n} + (0.1+j0.1)e^{3j(2\pi/10)n} + 0.2e^{5j(2\pi/10)n} \\ + (0.1-j0.1)e^{7j(2\pi/10)n} + (0.5+j0.25)e^{9j(2\pi/10)n}$$

Problems:

Chapter 8

Exercises:

8.3 Amp (V)=0.7071 V; phase=+135 degrees; RMS=0.5 V; Amp (dBV)=-6.0206 dBV.

8.4 0.6325 V; 0.4472 V; -6.9897 dB

8.14 +155 degrees.

8.19 0.3 kHz, 1.1 kHz, 2.1 kHz, 2.7 kHz, 3.3 kHz, 3.5 kHz, 3.9 kHz, 5.1 kHz, 5.3 kHz, 6.3 kHz, 7.1 kHz, 8.5 kHz, 9.5 kHz, 9.7 kHz, 11.5 kHz, 12.7 kHz, 15.9 kHz.

Problems:

8.10 Absolute Gains: 0.9984 V/V; 0.9475 V/V; 0.8881 V/V; 0.9362 V/V; 0.9871 V/V; 0.7269 V/V; 0.4469 V/V; 0.2291 V/V; Relative Gains: 0 dB; -0.4546 dB; -1.0169 dB; -0.5589 dB; -0.0990 dB; -2.7568 dB; -6.9824 dB; -12.7858 dB.

8.15 2nd order intermodulation frequencies: 0.8 kHz; 1.1 kHz; 1.9 kHz; 2.1 kHz; 3.2 kHz; 3.4 kHz; 4 kHz; 4.5 kHz; 5.3 kHz; 6.6 kHz; 7.4 kHz; 8.5 kHz; 3rd order intermodulation frequencies: 0.5 kHz; 0.6 kHz; 1 kHz; 1.1 kHz; 2.7 kHz; 2.9 kHz; 4.3 kHz; 4.7 kHz; 5.1 kHz; 5.5 kHz; 5.8 kHz; 7.4 kHz; 7.7 kHz; 7.9 kHz; 8.5 kHz; 9.3 kHz; 9.5 kHz; 11.7 kHz; 11.9 kHz; 12.7 kHz; 13.8 kHz.

8.17 (a) Noise = 65.0 uV RMS,

Chapter 9

9.13 2's complement DAC: $V_{MID} = 3.0159 \text{ V}$, $V_{DAC}(D = 101001) = 2.2857 \text{ V}$;
sign/magnitude DAC: $V_{MID} = 3.0 \text{ V}$, $V_{DAC}(D = 101001) = 2.7097 \text{ V}$.
Typographical error: Input digital code should be written as 101001.

9.26 $V_{noise} = 51.2 \text{ uV RMS}$; $SNR = 82.8 \text{ dB}$; $ENOB = 13.5 \text{ bits}$.

Chapter 10

Chapter 11

Chapter 12

Chapter 13

Chapter 14

Chapter 15

Chapter 16
