ECE 224a -- Syllabus

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ECE 224a is a VLSI project lab in which students construct designs which are submitted to MOSIS and subsequently tested. The course is “advanced” in that at least 1 prior VLSI class is required, and 2 are prefereable. The onus is not in the teaching of tools, but in design construction within a practical flow.

Topics:

Layout/Fabrication

Device Layout: contact, resistor, cap, transistor
Cell Layout: std. cell constriants, abstraction, LEF/DEF, scaling
Block Layout: Floorplanning and WirePlanning
Clock and Power Layout

VLSI Devices: MOS Transistors, Caps, Diodes, etc.

Device Variability: (sea of devices and moment reduction)
High Voltage: ESD, Driver, Guard Rings, Noise Mitigation, Rad Hardness

Analysis

Transient (Spice, couping, noise modeling, jitter)
Logical (Verilog, Static Timing, Power Analysis)
Transaction Level (C, system-C, Bluespec)

Data-Path and Memory Circuits

Static/Dynamic Memories
Ancillary Memory Analog Circuits

Analog Layout

Noise Issues: Substrate, Coupling, Power
Variability and Matching
Analog Device Layout