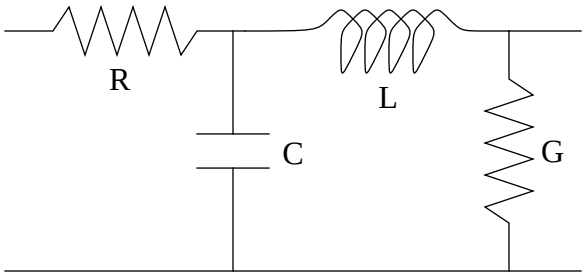
ECE 124d/256c
Lab1 (part a)

Due: Fri. Jan. 20, 2012 (1 week)

The write-up should be no more than 2-3 pages long and should be printed for grading, like your homework. There is a homework box as well as turn in during recitation.

Fig. 1



Transmission lines can easily be modeled with an incremental RLGC (also known as 'T') model as shown in fig 1. The values of R, C, G, and L are derived from the physical information surrounding the wire such as its width, height, length, material, and surrounding dielectric media, as well as other wires. You will need to choose a small length of wire which corresponds to a single iteration of the circuit model that provides reasonable accuracy in the simulation. If the segment is too long, the lumped approximation fails-- you get spurious results. If the segment is too small, the run times for the simulation and the models become very large.

Exp 1:

For this experiment, we are modeling a PCB trace. This trace is in 1oz copper, 15 mils wide. The trace is on the surface a 4 layer 0.032 inch thick PCB with a ground plane on each of the internal layers. The trace runs for 6 inches on the PCB and is un-terminated. (Yes -- in the US, PC boards are specified in inches/oz). The dielectric constant for the board is 4.2 and it has negligible conductance loss at these frequencies. Use the wire-over-ground-plane model found on the back cover of the textbook to figure out the inductance, resistance and capacitance for this wire. Drive this wire with a 0V to 3.3V rising edge of 250ps risetime (use a PWL waveform). To generate more realistic results, add a RC low pass filter at the source, to eliminate the higher frequency artifacts. Choose your R and C to give a corner frequency somewhere about 3GHz with R close to the parasitic impedance of the line. Run the experiment with the lumped segments representing 2cm, 1cm, 0.5cm, 0.25cm, 1mm and 0.5mm. Determine the coarsest spacing that gives you delays within 2% of what you expect from the TM model. What is the effective impeadance of the line?

Exp 2:

Using the same setup as above, apply an end termination resistor to the open line and document the results. Short the far end and re-run the test, also documenting the results. Simulate what would happen if the (un-terminated) wire was routed through a 1nH via 3 inches from the source

end. Repeat this test replacing the via with a copper pad that is 4mm x 2mm. Are the results what you expected?

Exp3:

On-chip wires typically run much faster than off-chip (use a rise-time of 25pS and RC corner of 50GHz), and they have much higher resistive losses. The wire is now 5mm long and on the redistribution layer of a 0.18µm technology, Cu based chip. This wire is 1.25µm thick, 7µm above the substrate, and 0.9µm wide. Instead of looking at just the ends of the wire for this experiment, plot the behavior of the wire at 1mm intervals. Because this rise time is approximately 10 times faster than the signal PCB trace we looked at, make sure that you divide the trace into appropriate segment lengths.