Epoch 3.2.2: Experiences of a First-Time User

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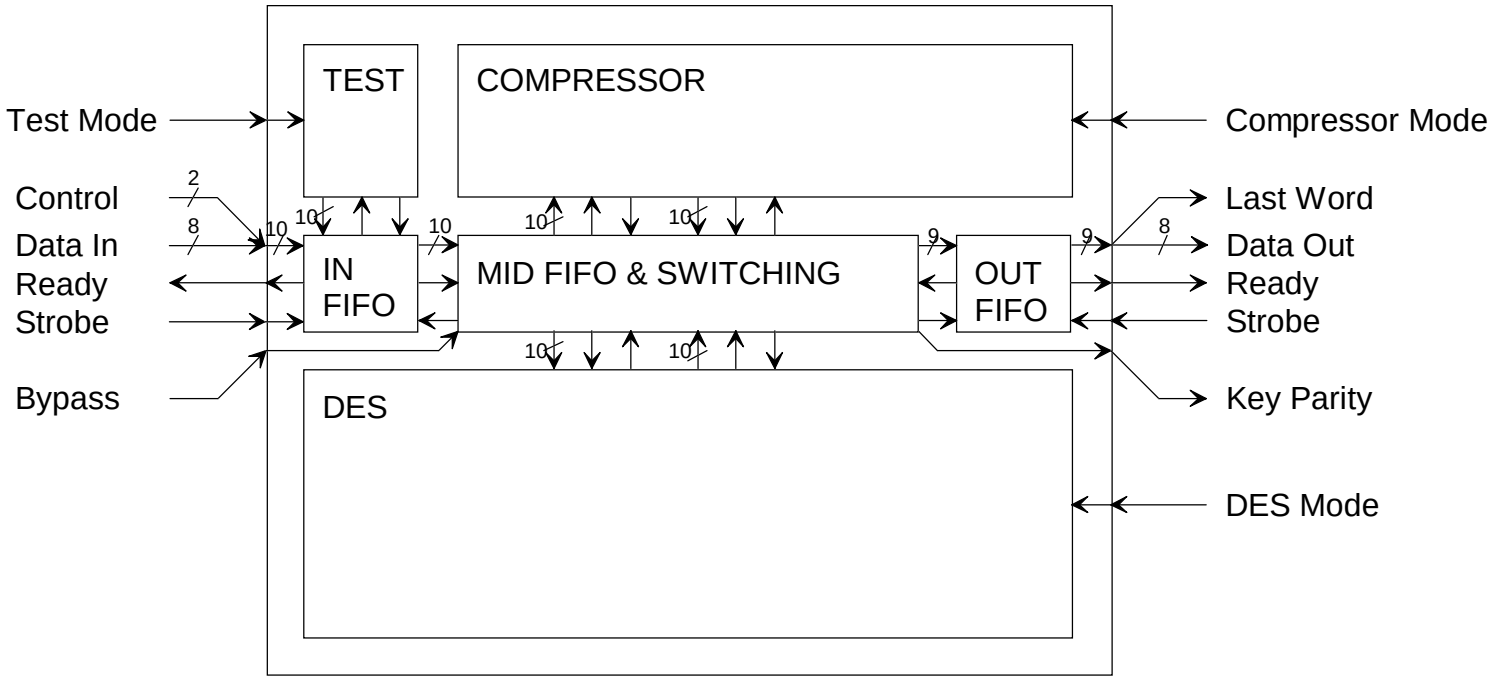
Motivations

- **Major Class Project**
  - **Data Compress/Encrypt-Decrypt/Decompress Chip**
    - **HP's CMOS26G 0.8 μm technology**
    - **Die size between 10 and 12 mm^2**
    - **Greater than 20 megabytes per second throughput**
    - **Epoch as primary CAD tool**
    - **Described in VHDL**
- **Best Design Fabricated**
- **First Real VLSI Design**

Outline

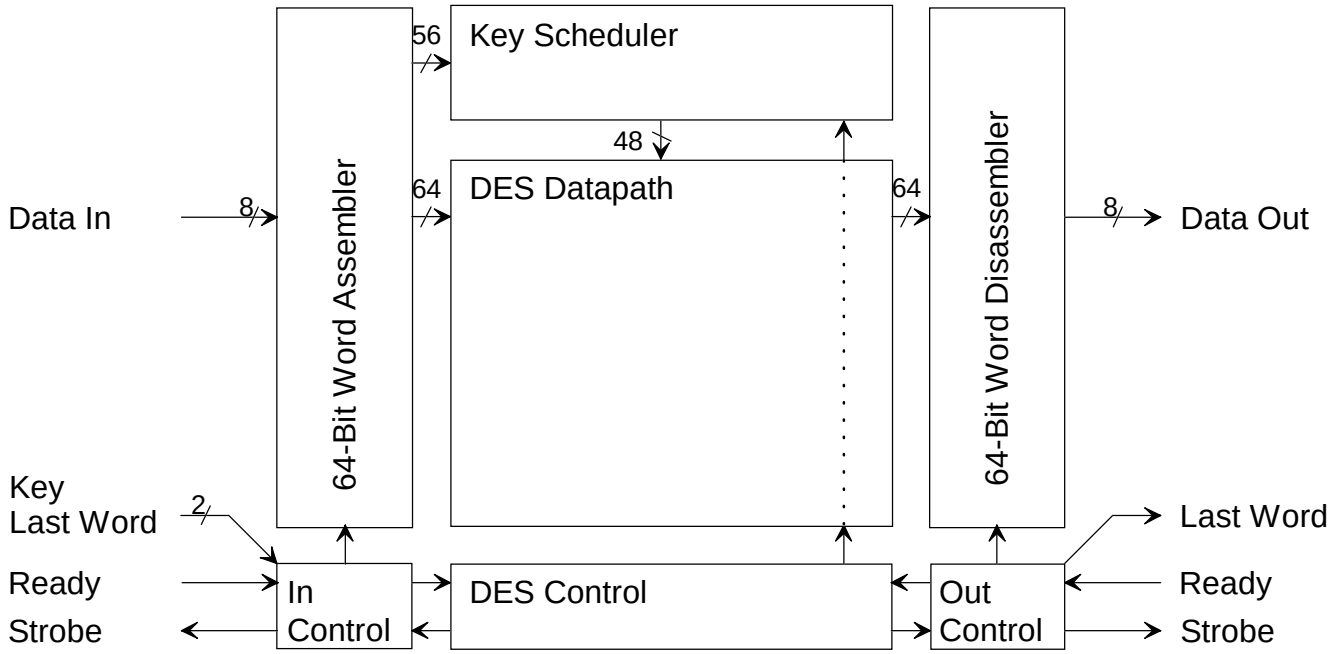
- Overview of the Rogue Chip
- DES
  - Block Diagram
  - Floorplanning
- Compression
  - Algorithm
  - Why This Compression?
  - Datapath
  - Power Rail Problems
  - Critical Delay
- Top-Level
  - Floorplanning
  - DRC Errors
  - LVS Errors
  - Simulation
- Conclusions

Rogue Chip Block Diagram



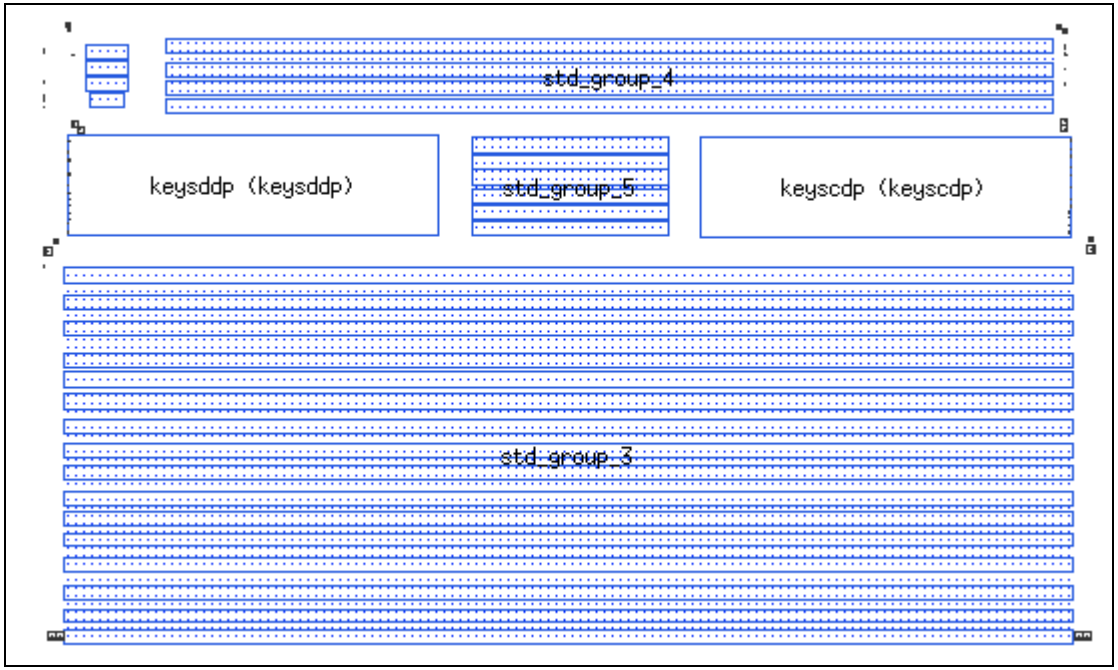
- **Straightforward operation**
- **4 modes**
- **Easy FIFO interfaces**
- **Lenient minimum clock skew**
- **Space saving 8-bit bandwidth**
- **Test LFSR versus scan**

DES Block Diagram



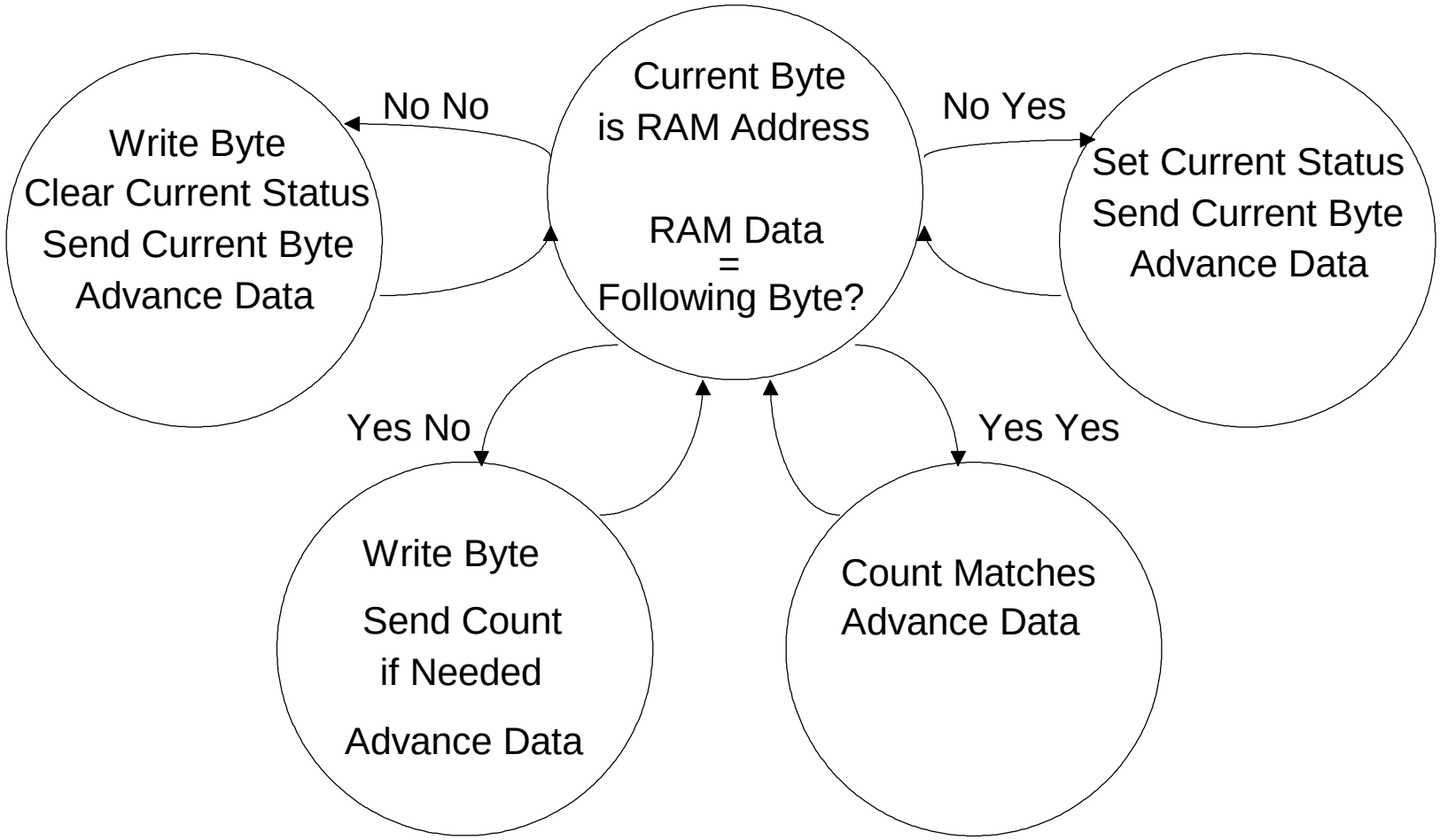
- **Three sections:**
  - **Assembler**
  - **DES**
  - **Disassembler**
- **16 Cycle DES**
- **Distributed control**
- **Lenient minimum clock skew**

DES Floorplanning



- **Difficult Floorplanning for DES**
  - **Hardwired permutations**
  - **32-bit crossing busses**
  - **Expansions and substitutions**
  - **No clear bit slices**
- **Forced manual placement**
- **Sparse datapath and large standard cell groups**
- **SIS generated S-Boxes**

Compression Algorithm



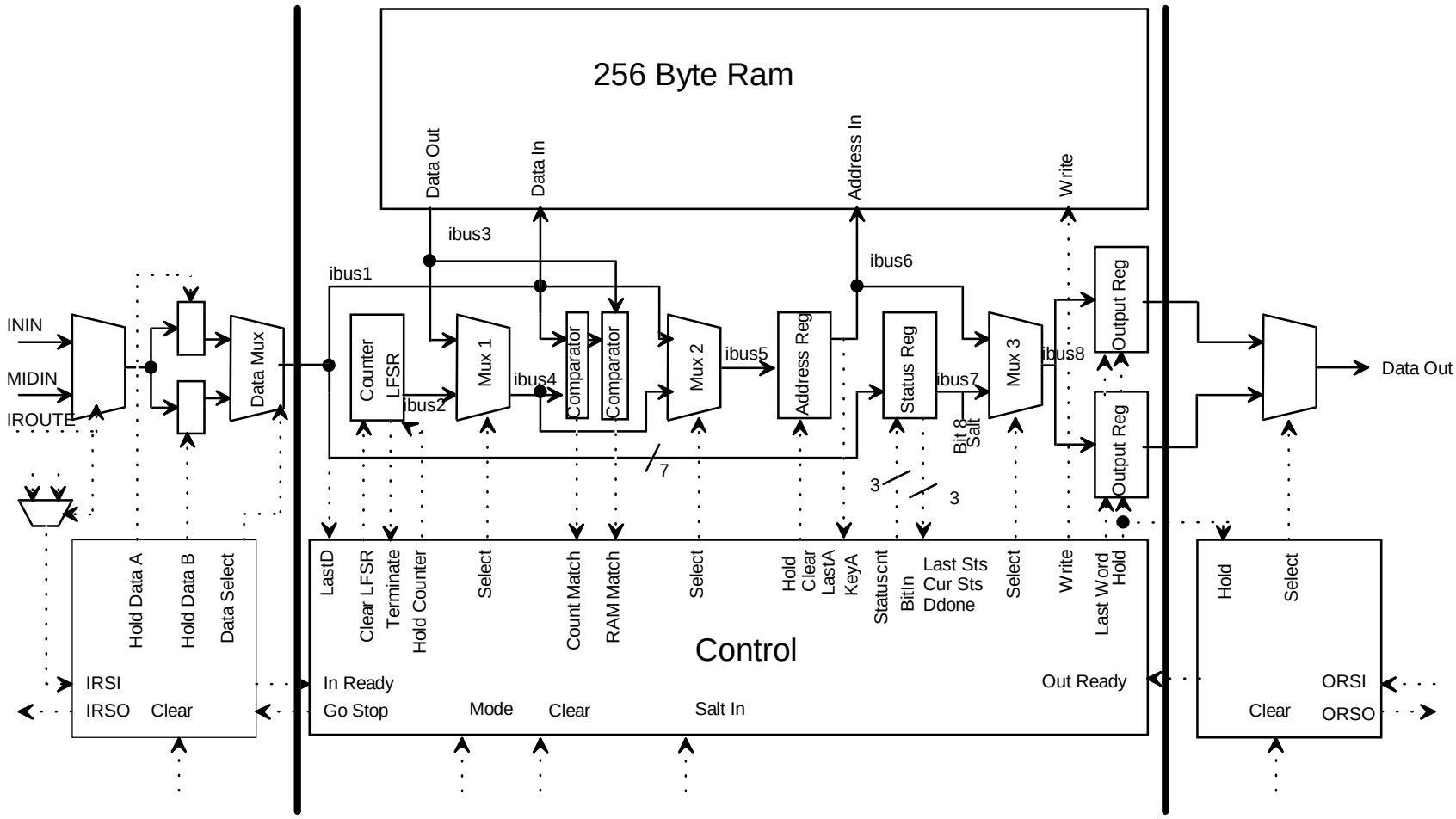
- **Generalization of run-length encoding**
- **Compressed data easily decompressed**

Why This Compression?

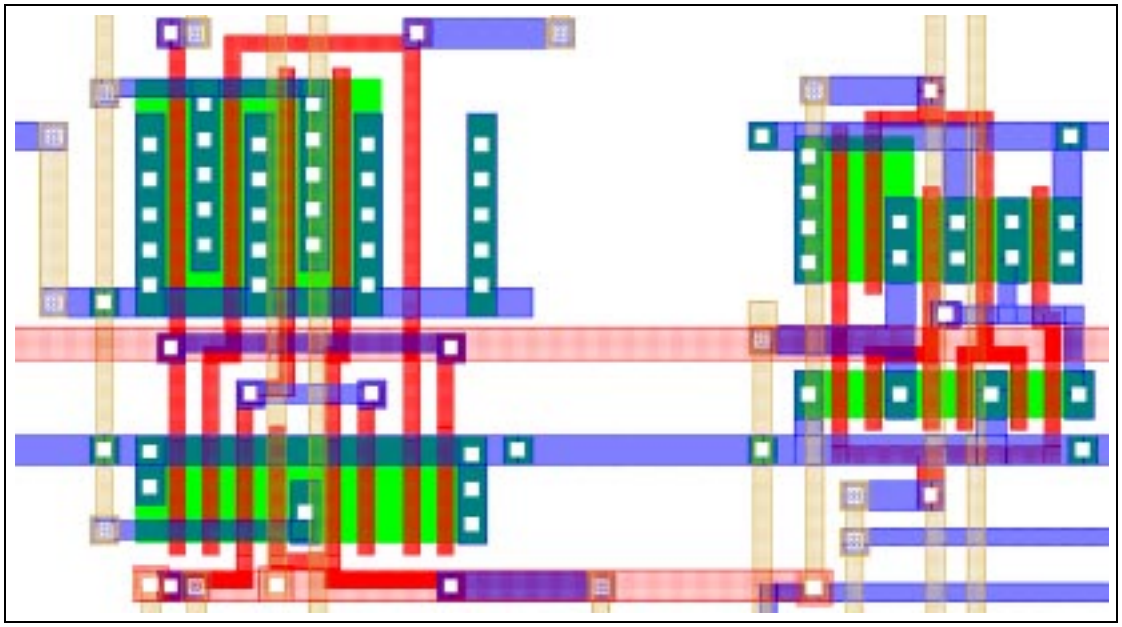
- **Small area requirement**
- **Closely matches DES' 1 byte every 2 cycles throughput**
- **Increases data entropy**
- **Provides reasonable compression**
  - **Typically 15-25% compression**
  - **Worst case 12.2% expansion**
  - **Best case 98.7% compression**

File	Compressed size as percentage of original size
TCW.EXE	74.3
README	92.3
DCOMP02.OBJ	86.5
TANGO2.ZIP	112.2
GEOBRN.WAV	105.7
CELLDD.CIF	83.5
QUAD.MAG	77.3
BEHERE.MID	94.7
VCR.BMP	81.6
MINISEC.PCB	78.4
SANTA1.WMF	76.5
TDW.EXE	89
SALETRAC.XLW	84.3
DESREG.VHD	80.3
400 ABCs	1.3

Compressor Datapath

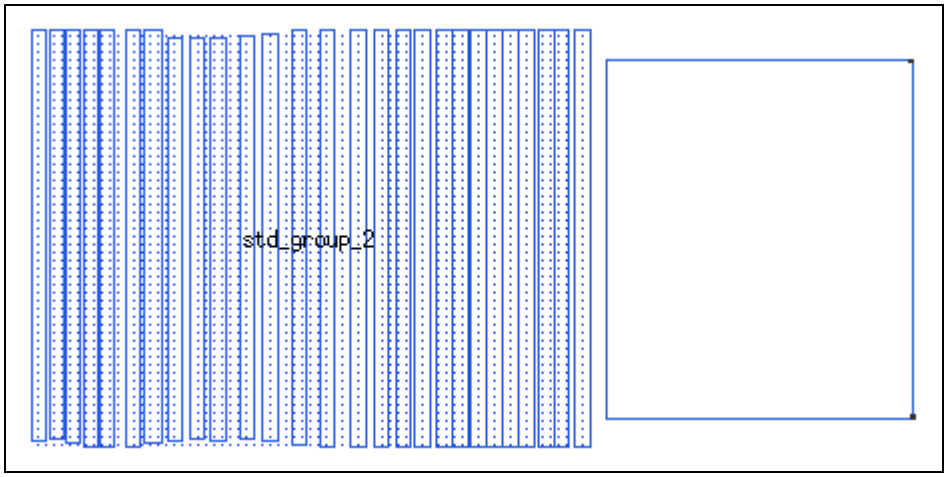


Compressor Power Rail Problems



- **Custom more compact arrangement of DP led to power rail opens**
- **Manually laying out compressor DP as standard cell group from within Epoch's floorplanner avoided DP power rail opens**
- **Resulting standard cell layout used less area than previous DP layout**

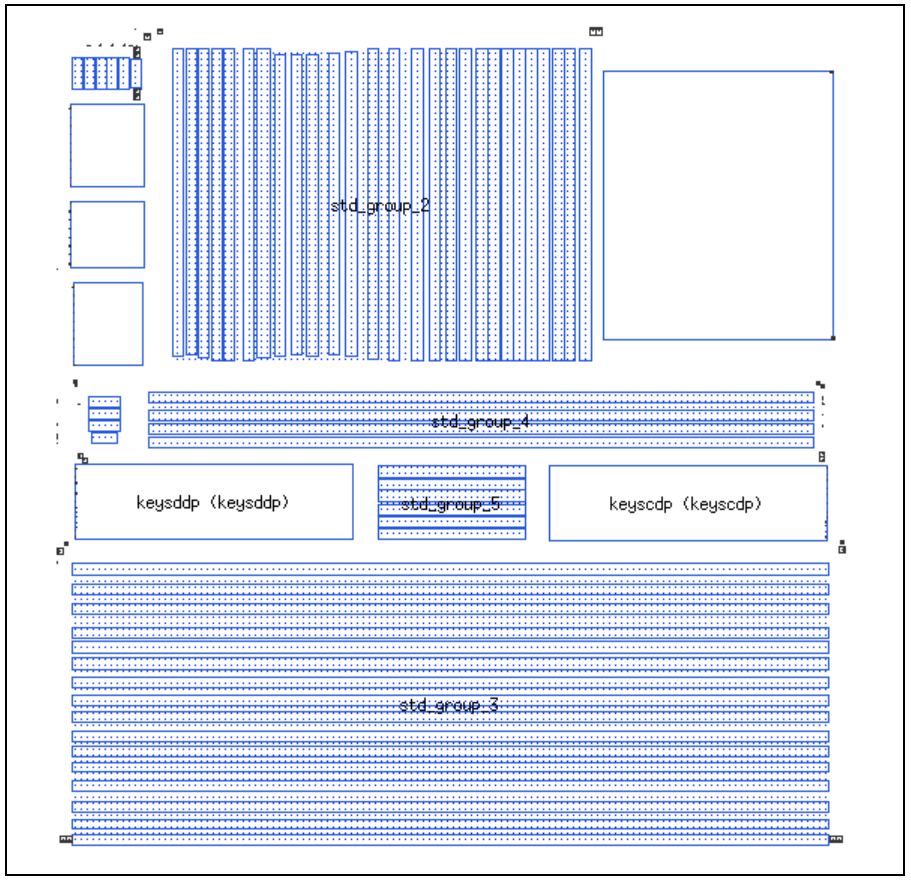
Compressor Control Critical Delay



- **Worst critical path greater than 12.5 ns**
- **Target frequency of 80 MHz unmet**
- **Met target frequency by:**
  - **Manually placing critical standard cells**
  - **Reducing non-critical buffer sizes**
  - **Rerouting**
  - **Timing-driven buffer sizing**

Top-Level Floorplanning

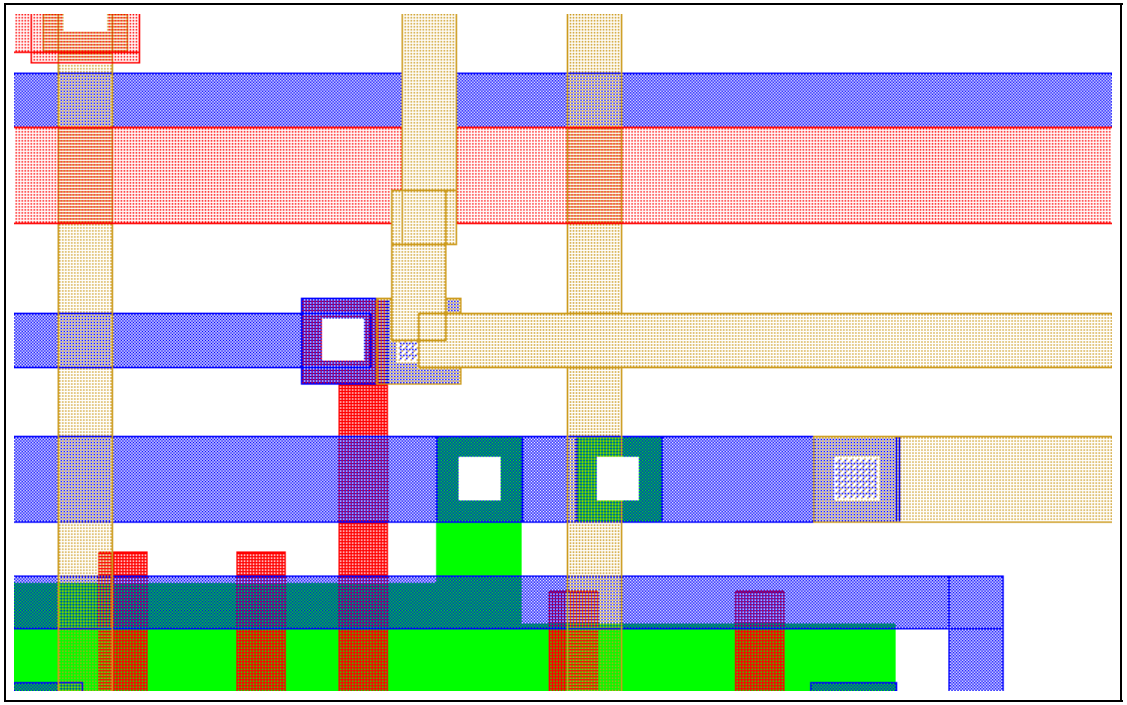
- **5.46×10^6 μm^2 core size after 30+ manual floorplanning sessions**
- **Area minimized by:**
  - **No general standard buffer sizing**
  - **Buffer sizing only on critical paths**
  - **Large standard cell groups**
  - **Reroute of entire chip from top level**
- **Automated results at least 50% larger**



DRC Errors

- **Checkmate's mask check revealed design rule errors**
  - **HP's design rules**
  - **Mainly metal-to-metal and metal-to-contact spacing errors**
- **Eliminated errors by slightly changing layout to force different route**

LVS Errors



- Checkmate's net check revealed layout versus schematic errors
- Mainly metal-to-metal shorts in glue and global routing
- Eliminated errors by manually specifying channels for offending routes

Chip Simulation

- **Complete SPICE electrical simulation awkward with 55,000 transistors**
- **Epoch generated VHDL model simulated with Mentor Graphic's QVSIM**
  - **VHDL model with timing data extremely helpful in identifying bugs**
  - **Tests included:**
    - Large file and random data test vectors
    - Random delays
    - Separate drifting clocks
- **Simulation failed to uncover design error**
  - **Race between FIFO strobe and mux select in compressor datapath**
  - **Differences in model timing and actual timing**
  - **No data setup or hold violations in FIFO models**
  - **Error verified with modified VHDL simulation**

Conclusions

- **DES working at 66 MHz**
- **Compressor crippled due to FIFO strobe and mux select race**
- **Shortcomings of Epoch 3.2.2 include:**
  - Opens in manually placed datapath power rails
  - Poor global placement
  - Shorts and design rule errors
  - No engineering change tools
  - No timing-driven standard cell placement optimization
  - No data setup and hold violations on FIFO models

Conclusions

- **Strengths of Epoch 3.2.2 include:**
  - Manual modification freedom
    - Floorplanning
    - Buffer Sizing
  - Versatile and quality simulation output
    - TACTIC
    - VHDL with timing data
  - Exceptional circuit management and design ease
    - Essentially one first-time VLSI designer
    - 6 months part-time effort
    - 55,000 transistors in 10.6 mm^2
    - Working DES