

7. Introduction to mixed-signal testing using the IEEE P1149.4 standard

It was already mentioned in previous chapters that the IEEE 1149.1 standard (BST) was developed with the specific purpose of addressing the structural test of printed circuit boards. The narrow scope of BST simplified its acceptance and helped to accelerate the introduction of BST products, since there were few compromise solutions requiring an agreement among the sectors involved (the design and test community, semiconductor and ATE manufacturers, CAD companies, etc.). The effectiveness of this test technology was a strong contributor to its success, but it takes more than a good solution to gain market acceptance. On the other hand, its narrow scope meant that a reasonable number of problems would remain in the queue waiting for a broader solution. One of the areas which was left behind was the testing of mixed-signal circuits, which became a visible R&D trend in recent years due to the increased market share of this type of products. One of the most promising approaches towards an effective mixed-signal test technology is the P1149.4 standard, which will be presented in this chapter.

7.1 Scope of the IEEE P1149.4 standard

The proposed 1149.4 (P1149.4) IEEE standard is expected to be approved in the near future and consists of an extension to 1149.1, defining the structures that are to be added to an 1149.1-compliant chip, in order to simplify the testing of mixed-signal circuits.

It is important to stress the fact that the P1149.4 infrastructure, being an extension to BST, widens its application domain, but keeps exactly the same characteristics of a serial access scan infrastructure. This means that areas such as functional testing will still be insufficiently served by this new test technology, because of the serial nature of scan and also due to the difficulty of synchronising functional events and test operations. However, the structural test operations enabled by the BST infrastructure will now be able to address mixed-signal circuits as well. Moreover, some parametric test operations will now become possible, such as measuring the impedance of discrete components placed

between P1149.4 pins, or checking the DC threshold levels in digital circuit inputs and outputs.

The introduction of P1149.4 may therefore be seen as an important extension of the original 1149.1 concept, even if still very much restricted to structural test. The addition of optional instructions to 1149.4-compliant circuits will however enable wider application areas, eventually including hardware debugging, functional test operations and real-time fault detection (such as is already possible with enhanced 1149.1 infrastructures).

7.2 P1149.4 Overview

In this section we will present an overview of P1149.4, stressing the common features to 1149.1 and pointing out the main differences (and their implications) between these two test infrastructures.

7.2.1 The basic P1149.4 architecture

The additional structures defined by P1149.4, as compared to those defined in 1149.1, are the following:

- An Analog Test Access Port (ATAP) with two pins (AT1 and AT2). AT1 will normally be used to drive analog values into the core circuitry or analog pins, and AT2 used to monitor the responses to analog stimulae (the conceptual solution described in the P1149.4 draft document would allow AT1 and AT2 to reverse their roles).
- An internal analog test bus consisting of at least two lines (AB1 and AB2), which is used to route analog stimulae into and out of the chip (core circuitry or analog pins)
- A test bus interface circuit (TBIC), inserted between the ATAP pins and the internal analog test bus, which defines the type of connections and signals present in these analog lines
- Analog boundary modules (ABM), inserted between analog pins and core circuitry. The boundary modules are the P1149.4-equivalent of BS cells, which in P1149.4 are called ABMs and DBMs (digital boundary modules, in this case associated with digital I/O pins). Except because of overhead

concerns, ABMs might also be inserted between digital pins and their core circuit connections.

The basic P1149.4 architecture may be represented as illustrated in figure 7.1, where the four additional structures referred above are shown.

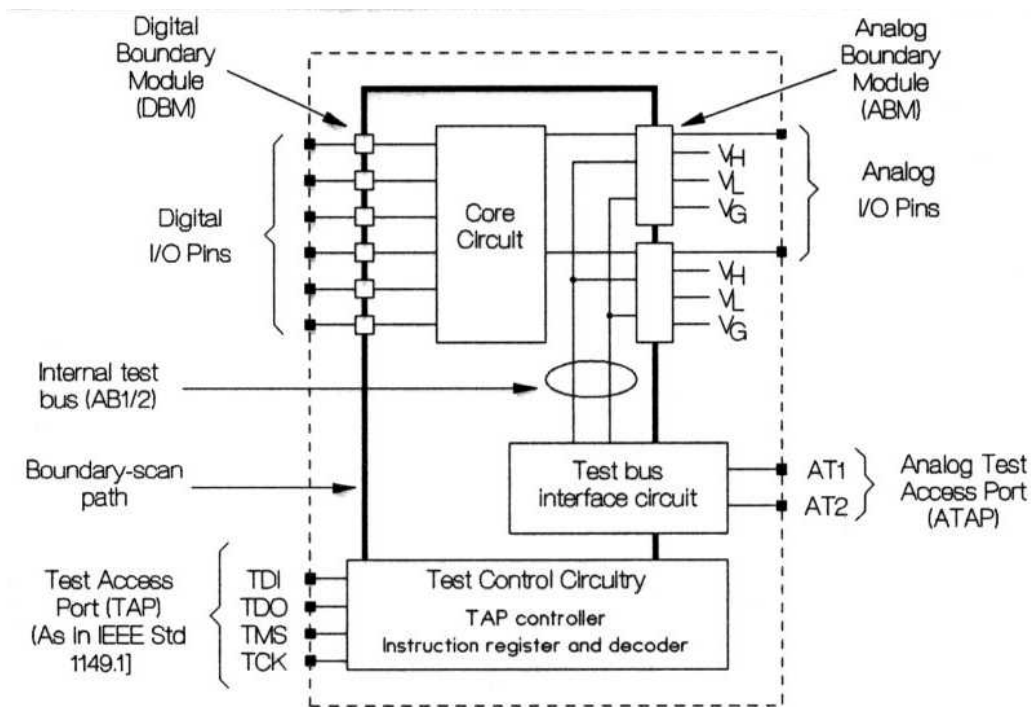


Figure 7.1: The basic P1149.4 architecture.

Each analog I/O pin has an associated ABM that provides extended controllability and observability operations, enabling interconnect testing and certain types of parametric testing operations. Notice also that ABMs and DBMs are serially connected in an extended boundary scan (BS) register, which also includes cells belonging to the TBIC (as will be described later). Apart from the additional structures referred, the overall test architecture is clearly identical to 1149.1, as would be expected.

The operation of the P1149.4 infrastructure may be summarised as follows:

- An analog input is externally applied to AT1 and the analog output is monitored at AT2
- AT1 and AT2 are connected to the two-wire internal test bus, respectively to AB1 and AB2
- From AB1 the signal can be routed to the core or to a function output pin

- Responses are routed to AB2 from the core or from a function input pin

7.2.2 P1149.4 test register structure

The P1149.4 architecture may alternatively be represented as shown in figure 7.2, which emphasises the test registers present.

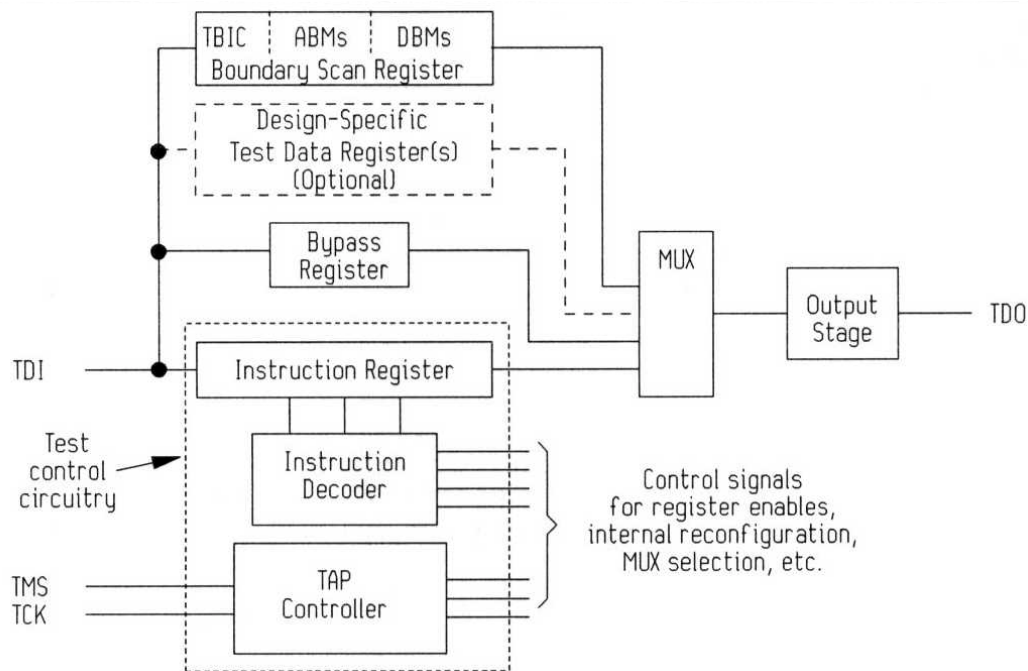


Figure 7.2: P1149.4 test register structure.

Figure 7.2 shows that the register architecture of P1149.4 is entirely digital and essentially identical to the one defined by 1149.1. The BS register comprises the control registers of the TBIC and the ABMs, which are used to define their respective operating modes.

7.2.3 P1149.4 instructions

Besides the three mandatory 1149.1 instructions, P1149.4 defines a fourth mandatory instruction called PROBE. The functionality of the PROBE instruction may be summarised as follows:

- The selected data register is the BS register
- Each ABM will connect its pin to the core circuitry
- AT1 and AT2 are connected to AB1 and AB2

- Connection between the analog I/O pins and AB1 / AB2 is defined according to the control register in each ABM
- Each DBM operates in transparent mode (as if SAMPLE / PRELOAD or BYPASS were the current instruction)

In relation to the three mandatory instructions common to 1149.1, the following additional P1149.4-specific rules apply:

- For BYPASS and SAMPLE / PRELOAD: i) AT1 / AT2 must be isolated from AB1 / AB2, as well as from all test voltage sources; ii) all analog function pins must be connected to the core circuit; iii) all analog function pins must be isolated from AB1 / AB2 and from all test voltage sources.
- For EXTEST: The ABMs must disconnect the pin from the core circuit.

Optional P1149.4 instructions are the same as for 1149.1 (INTEST, ID / USERCODE, RUNBIST, CLAMP and HIGHZ) and have a similar description, to which are appended the rules applying to the operating modes of the TBIC and ABMs.

7.3 P1149.4: The main blocks

The basic architecture of P1149.4, illustrated in figure 7.1, shows that two main blocks were added to the original 1149.1 test infrastructure, respectively the TBIC and the ABMs. These blocks assure the main feature of P1149.4, which is the application and monitoring of analog test signals. Each of these blocks comprise a switching architecture (defining the interconnection among their I/O signals) and a control structure (which defines the operating mode of the switching architecture), that will now be analysed in detail.

7.3.1 The Test Bus Interface Circuit (TBIC)

The TBIC controls the connections between the ATAP and the internal analog test lines. The draft P1149.4 document specifies that there must be at least two internal analog test lines, AB1 and AB2, as was shown in figure 7.1. When this is the case, the switching architecture of the TBIC may be represented as shown in figure 7.3.

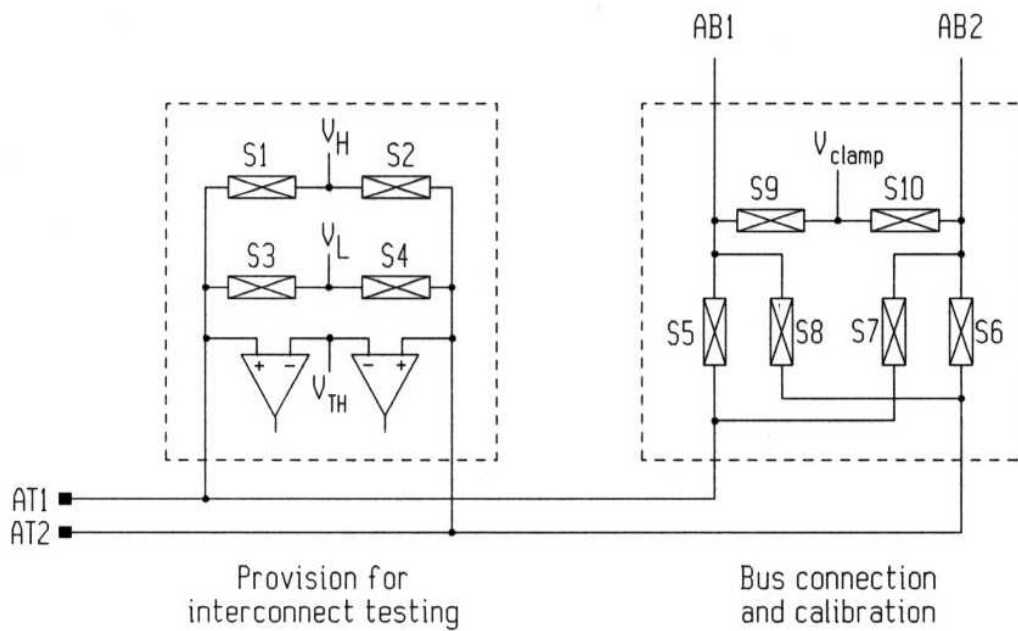


Figure 7.3: Switching architecture of the TBIC.

The ten switches shown in figure 7.3 (S1 to S10) define the signals that will be present in the ATAP pins and the internal analog test bus lines. Notice in particular that the switching architecture of the TBIC allows:

- AT1 or AT2 to be connected to V_H or V_L
- AT1 or AT2 to be connected to AB1 or AB2
- AT1 or AT2 to be connected to the internal voltage source V_{CLAMP}
- A 1-bit representation of the voltage at AT1 or AT2 (as compared to the threshold voltage V_{TH})

The condition (on / off) of the switches shown in figure 7.3 is defined by the TBIC control structure. Since not all possible combinations are useful (or legal), four bits are sufficient to select the required operating mode, as illustrated in figure 7.4 (the current draft specification describes only ten switch combinations, which are able to satisfy the basic requirements set up for the TBIC).

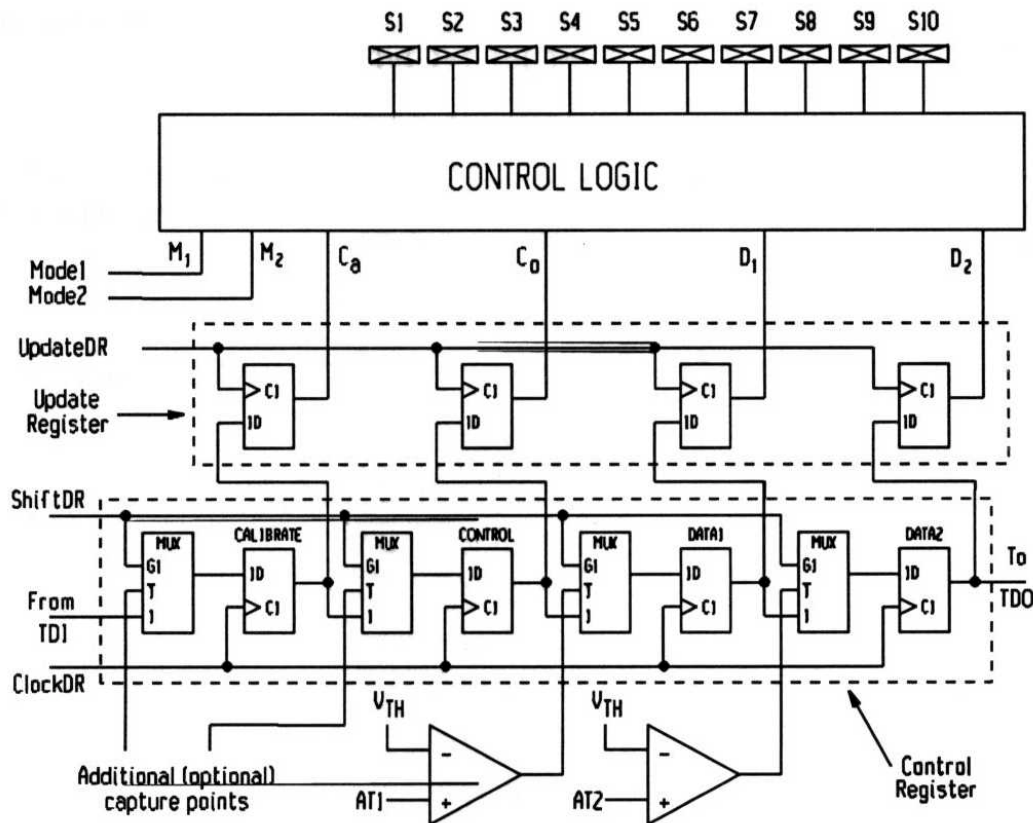


Figure 7.4: Control structure of the TBIC.

The TBIC control structure forms part of the BS register and its description may be summarised as follows:

- It comprises four cells (bits), each one with a capture / shift stage and an update stage. Notice that these cells are not significantly different from the typical configuration found in standard 1149.1 BS cells. The main difference is the absence of an output multiplexer, which is not required here because these cells have no (external) parallel input to the update stage.
- The four bits in the capture / shift stage are called CALIBRATE, CONTROL, DATA1 and DATA2. DATA1 and DATA2 capture the 1-bit representation of the voltages at AT1 and AT2, as compared to V_{TH} , while CALIBRATE and CONTROL are available as additional capture inputs for design-specific circuit conditions.
- The four bits in the update stage, together with the instruction decoder outputs MODE1 and MODE2, define the operating mode of the TBIC switching architecture

7.3.2 The Analog Boundary Modules (ABM)

The ABMs are the heart of the P1149.4 architecture. Test signal application and response capturing through the ABMs takes place by combining serial access to the BS register and analog stimulae access to the ATAP. Similarly to the TBIC, the ABMs comprise a switching architecture and a control structure to define the flow of analog signals into and out of the function pins. The switching architecture of each ABM is represented in figure 7.5.

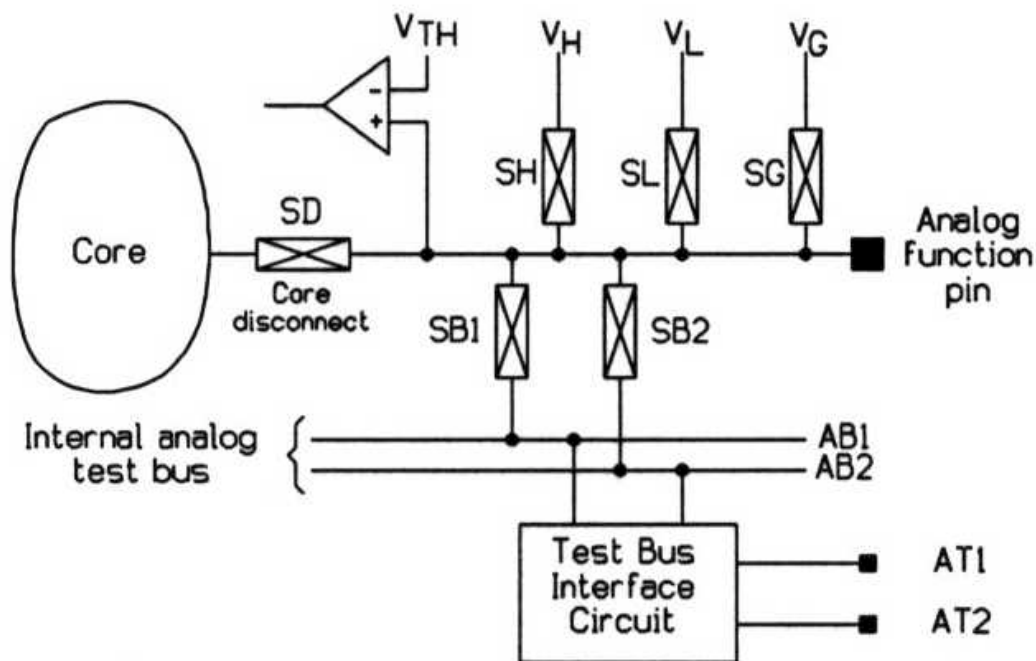


Figure 7.5: Switching architecture of the ABMs.

The switching architecture shown comprises six switches that are combined to provide the following functions:

- To disconnect the core from the function pin
- To drive the pin from AB1 (controllability)
- To drive AB2 from the pin (observability)
- To monitor a 1-bit representation of the voltage on the pin (as compared to V_{TH})
- To connect V_H or V_L to the pin (for interconnect test)
- To connect a reference quality voltage (V_G) to the pin (useful for parametric measurements)

The control structure of each ABM may be represented as shown in figure 7.6.

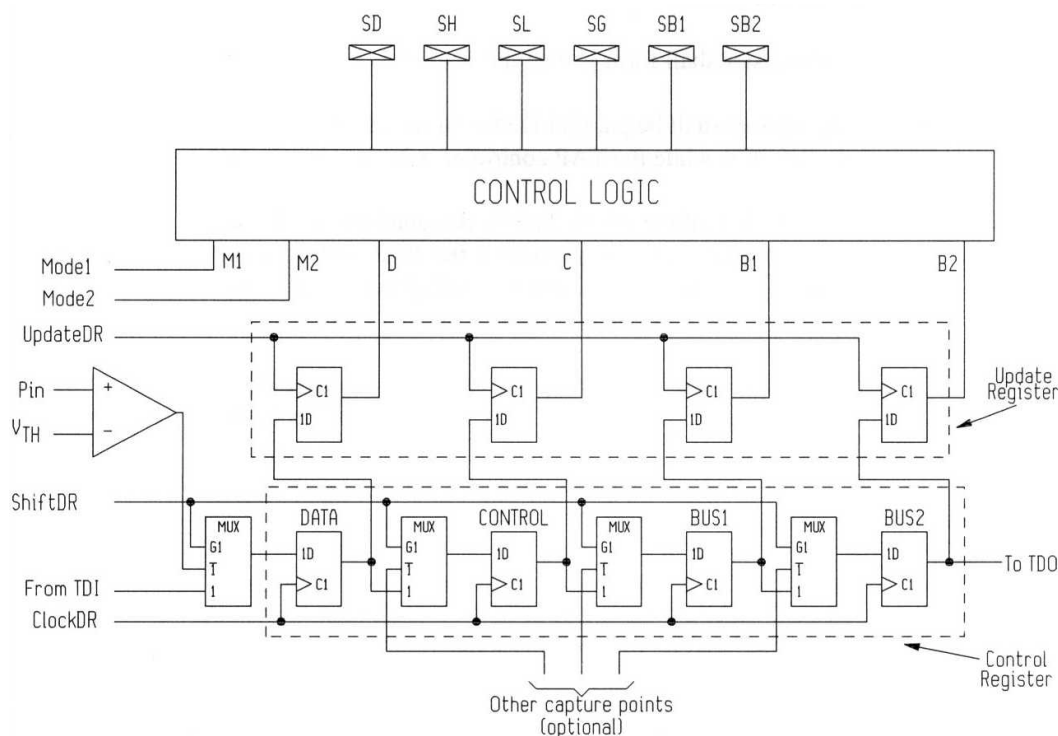


Figure 7.6: Control structure of the ABMs.

The control structure for the ABMs is similar to the same structure in the TBIC and may be summarised as follows:

- It comprises four cells (bits), each one with a capture / shift stage and an update stage, exactly as shown for the TBIC control structure.
- The four bits in the capture / shift stage are called DATA, CONTROL, BUS1 and BUS2. DATA captures the 1-bit representation of the voltage at the function pin, as compared to V_{TH} , while the other bits are available as additional capture inputs for design-specific circuit conditions.
- The four bits in the update stage, together with the instruction decoder outputs MODE1 and MODE2, define the operating mode of the ABM switching architecture

7.4 Interconnect testing with P1149.4

The detection of open or short-circuit faults with P1149.4 is similar as with 1149.1 and may be summarised as follows:

- In the case of digital pins, the data is loaded directly into the DBMs
- In the case of analog pins, the control codes that cause internally generated voltages (V_H or V_L) to be applied to the pins are loaded into the ABMs
- Test vector application and response capturing starts with the SAMPLE / PRELOAD instruction to shift in the first test vector and deals only with digital data (both for digital and analog pins)

It is particularly important to emphasise the fact that interconnect testing uses only digital test vectors, even for analog pins, and is based exactly in the same algorithms used for digital-only circuits, since:

- The high (V_H) and low (V_L) voltages applied to analog function pins are generated internally
- V_H or V_L are applied to the analog output pins as defined by the data shifted into the control structure of the ABMs
- The responses present at each analog input pin are converted to digital through the comparator present in the switching structure of the ABMs and read into the DATA bit in the capture / shift stage of the ABMs control structure

Notice also that interconnect testing does not use the ATAP pins, which are only necessary when analog signals are to be applied or captured (and namely in parametric testing), as will be shown in the following section.

7.5 Impedance measurements with P1149.4

Impedance measurements require the use of the ATAP pins, together with the TBIC and ABMs, to apply and read analog test stimulae. Two examples of impedance measurement will be considered, as presented in the draft P1149.4 document, where additional examples may be found.

7.5.1 Impedance between pin and ground

The measurement of an impedance between a pin and ground may be done using the set up shown in figure 7.7.

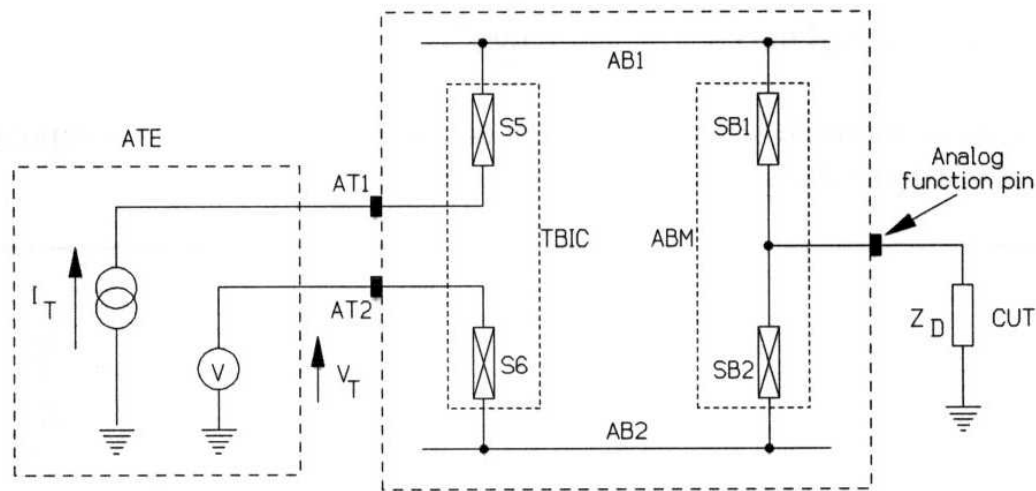


Figure 7.7: Test set up for measuring an impedance between pin and ground.

The measurement procedure may be summarised as follows for this case:

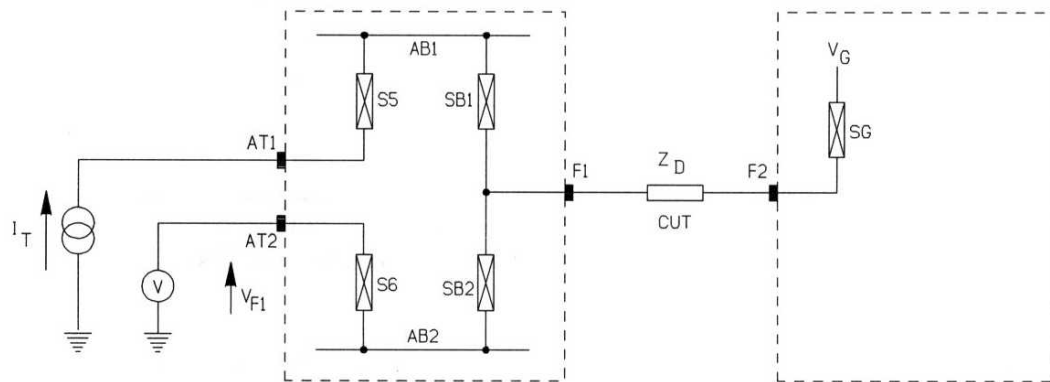
- A known current I_T is applied through AT1, by way of switches S5 and SB1, to the unknown impedance (Z_D)
- The resulting voltage V_T is measured at AT2, which is connected to Z_D through switches SB2 and S6
- The value of Z_D may then be computed as $Z_D = V_T / I_T$

Notice that the error margin in this procedure depends on the relative values of the unknown impedance (Z_D), the voltmeter input impedance (Z_V) and the impedance of each switch in the measurement path. The value obtained for Z_D will only be acceptable if the following assumptions are valid:

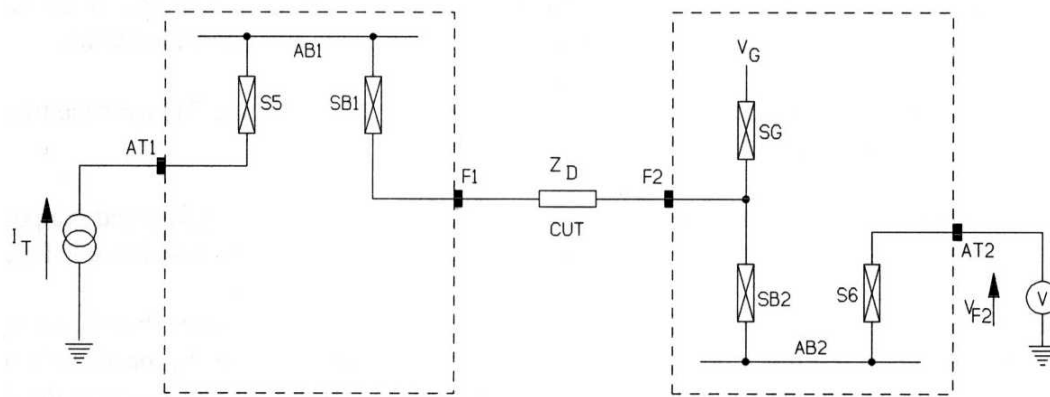
- $Z_V \gg Z_{S6} + Z_{SB2}$ (to guarantee that the voltage drop in S6 and SB2 is negligible)
- $Z_V + Z_{S6} + Z_{SB2} \gg Z_D$ (to guarantee that the percentage of I_T which does not flow through Z_D is negligible)

7.5.2 Impedance between two pins

The measurement of an impedance between two pins may be accomplished with the test set up shown in figure 7.8. Notice that the values of I_T and V_{F1} resulting from the first measurement would suffice to determine Z_D , assuming that V_G is known. However, if a second measurement is made, the value of Z_D may be determined without knowing V_G .



(a) First measurement (V_{F1}).



(b) Second measurement (V_{F2}).

Figure 7.8: Test set up for measuring an impedance between two pins.

The first part of the measurement procedure is illustrated in figure 7.8.a and consists of the following steps:

- A known current I_T is applied through AT1, by way of switches S5 and SB1, to the unknown impedance (Z_D), that has a fixed voltage V_G applied at the other end
- The resulting voltage V_{F1} is measured at AT2, which is connected to Z_D through switches SB2 and S6
- The fact that V_G is a high quality reference voltage guarantees that the flow of I_T will not cause any significant change in its voltage output

The second part of the measurement procedure is illustrated in figure 7.8.b and consists of the following steps:

- Current I_T is again applied through AT1, by way of switches S5 and SB1, to the unknown impedance (Z_D), that continues to have voltage V_G applied at the other end
- The resulting voltage V_{F2} is measured at AT2 of the second P1149.4-compliant component, which is connected to Z_D through switches SB2 and S6
- The value of Z_D may now be computed as $Z_D = (V_{F1} - V_{F2}) / I_T$

Notice that the error margin in this new procedure continues to depend on the relative values of the various impedances present in the measurement path (including Z_{SG}). Assuming that Z_{SG} is very low (a reasonable assumption, since V_G is a reference quality voltage source), then the value obtained for Z_D will be acceptable if the following assumptions are valid:

- Regarding the first measurement (V_{F1}), in figure 7.8.a, the same assumptions already referred (to measure Z_D between pin and ground) apply as well
- As for the second measurement (V_{F2}), in figure 7.8.b, it is required that $Z_V \gg Z_{S6} + Z_{SB2}$ (to guarantee that the voltage drop in S6 and SB2 is negligible in the second P1149.4 component)

7.6 P1149.4: Further information

There are several sources of information available concerning the IEEE P1149.4 standard for mixed-signal testing. Due to the usefulness of web-based electronic references, one of the most important resources for this purpose is the web page of the P1149.4 Working Group, shown in figure 7.9, which can be reached at URL <http://grouper.ieee.org/groups/1149/4/index.html>.



Figure 7.9: Home page of the IEEE P1149.4 Working Group.

Another important resource in this area is the web page of the NORMATE initiative (Network of researchers in mixed-signal and analogue testing), illustrated in figure 7.10, which can be reached at URL <http://normate.tet.uni-hannover.de/public/about.html>.

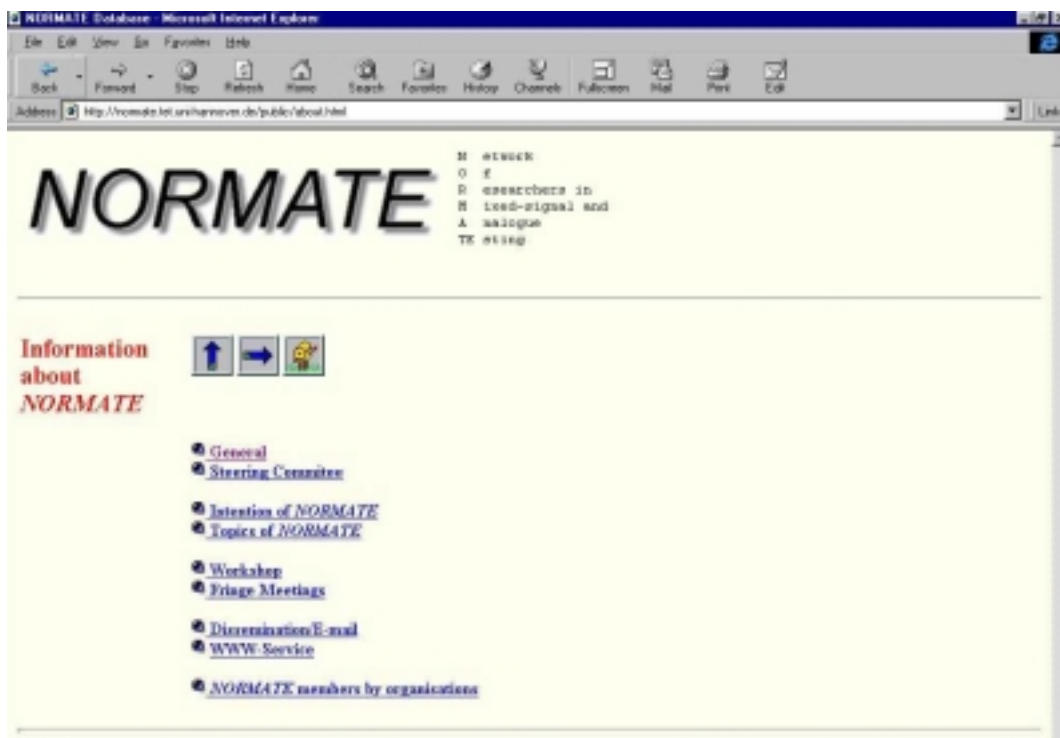


Figure 7.10: Home page of the NORMATE initiative.

Concerning printed material, the main source of information is the P1149.4 draft document: *P1149.4 / D19 Draft Standard for a Mixed-Signal Test Bus*, prepared by the Mixed-Signal Working Group of the Test Technology Technical Committee of the IEEE Computer Society (March of 1998).

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