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Description

Our project goal is to implement an analog to digital Delta-Sigma converter that is targeted at a bandwidth from of 20 kHz. A switched capacitor second-order front-end will be used along with a digital filtering scheme on the back end.

Changes from Original Specifications

The oversampling rate has been reduced from 512 to 256. This was because tones were observed in the noise spectrum at higher OSR's (Figure 4 vs. Figure 3). This somewhat eases the requirements on the digital filters. On the other hand, the output bit width has been increased substantially to 16 bits. Thus, we intend to stick with the initial proposal of sinc3 decimation by 64 followed by 2 half band filter stages. Some investigation revealed certain half-band structures [1] that are created as cascaded identical sub-filters. The work itself is outside our grasp, but we have a toolbox that lets us design filters of this topology. This essentially reduces the number of coefficients needed by a huge amount.

Front End Architecture – System Model

The general topology of the front end was analyzed using Simulink. The model was adapted form Brigatti et.al. [2] This allowed us to analyze trade-offs between system specifications, and system variables. In addition to system parameters noise models for kT/C noise, sampling jitter, and amplifier swing constraints (maximum operating voltage, slew rate) were added to the model (Figure 1). With the addition of this a change in the amplifier behavior could be quickly simulated and accounted for before a global spice simulation had to be run. Using this model allowed us to view several problems before actually implementing the circuit, the most notable of which introduced tones for the highest oversampling ratios.

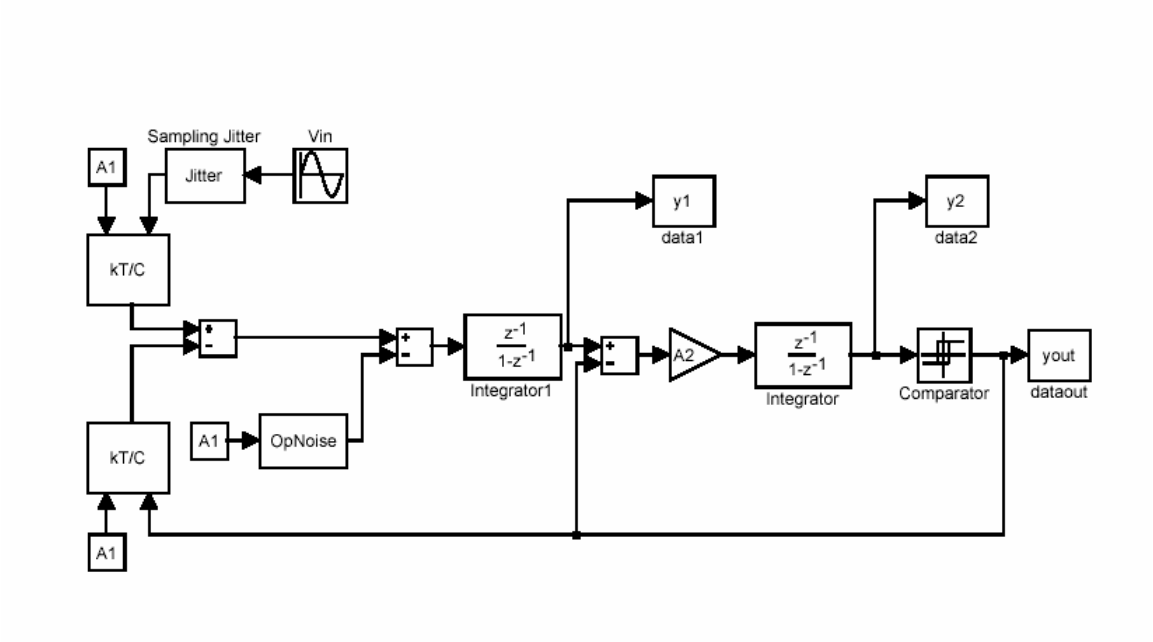


Figure 1: Simulink model

The model above was used to run several simulations with varying operational conditions. A slew rate of $20*10^6$ V/s was assumed, and a clock jitter of 1 ns was assumed. Using these specs we were able to achieve 15.6 effective bits, and signal to noise ration of 95.6 dB (Figure 2). If we assumed a slightly more realistic jitter of 100 ps, and a slightly higher comparator slew rate we were able to push up the number effective bits to 16. However, even with the improved assumptions we were not able to improve the excess tones that occur at an oversampling rate of 512. To ease the requirements on the back end filter we decided to decrease the OSR from 1024 down to 256.

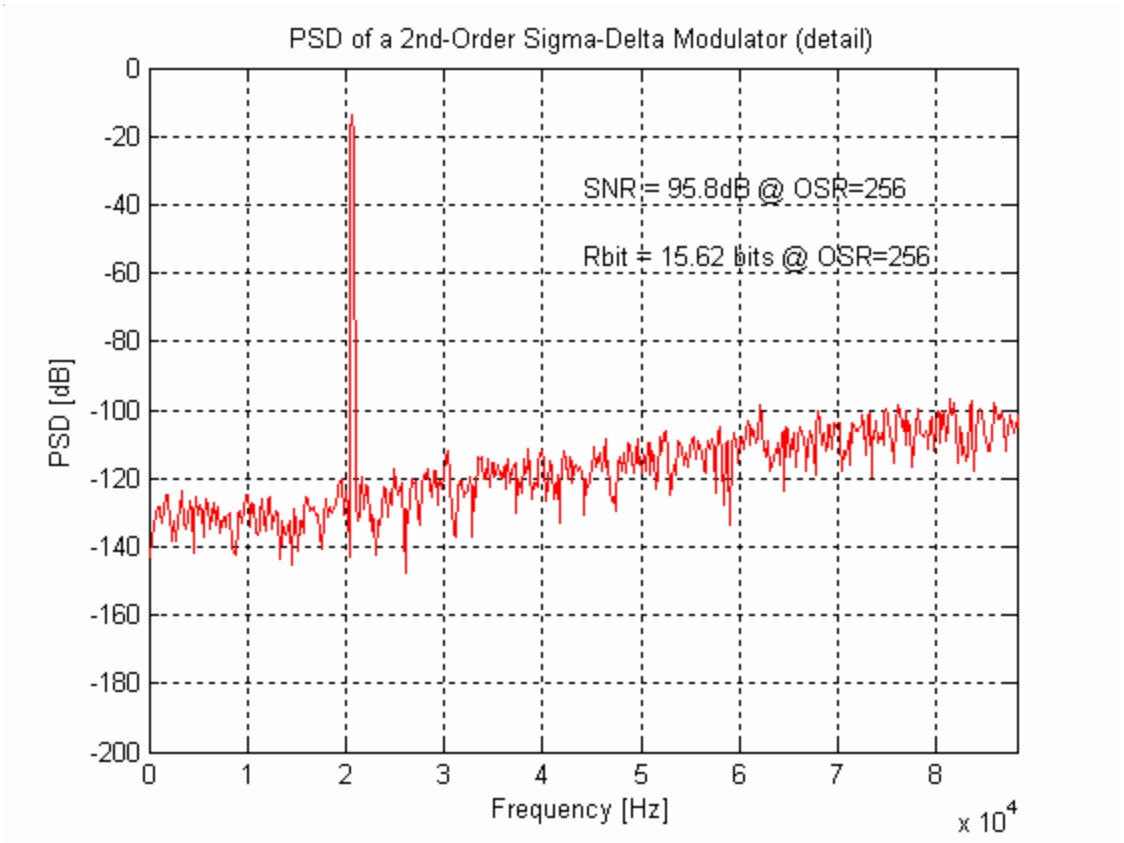


Figure 2: Power Spectral Density of Lower Band with OSR = 256.

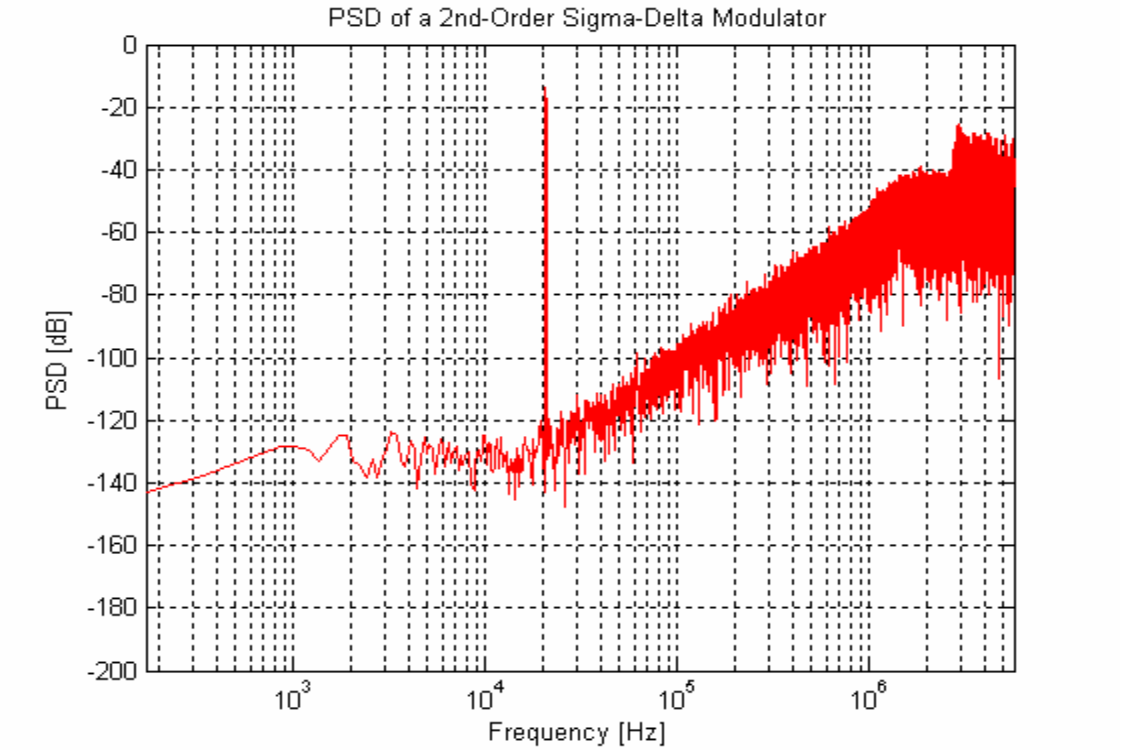


Figure 3: Power Spectral Density on Log Scale with OSR = 256.

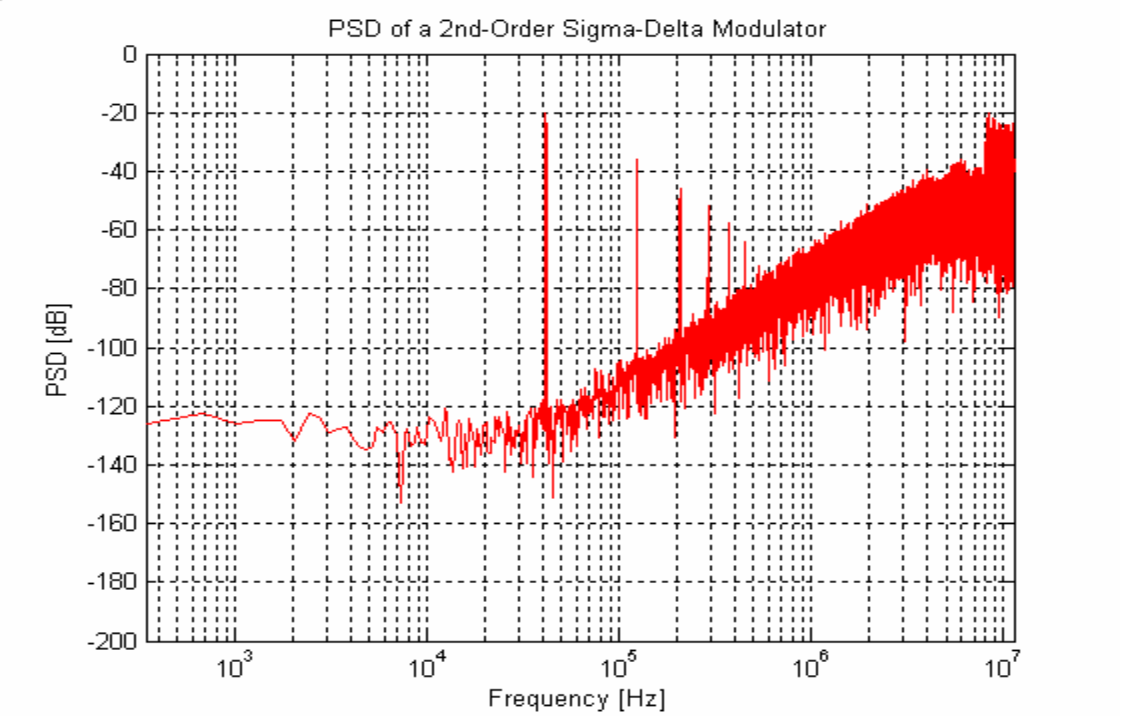


Figure 4: Power Spectral Density to 6 MHz on Linear Scale with OSR = 512 showing excess tones.

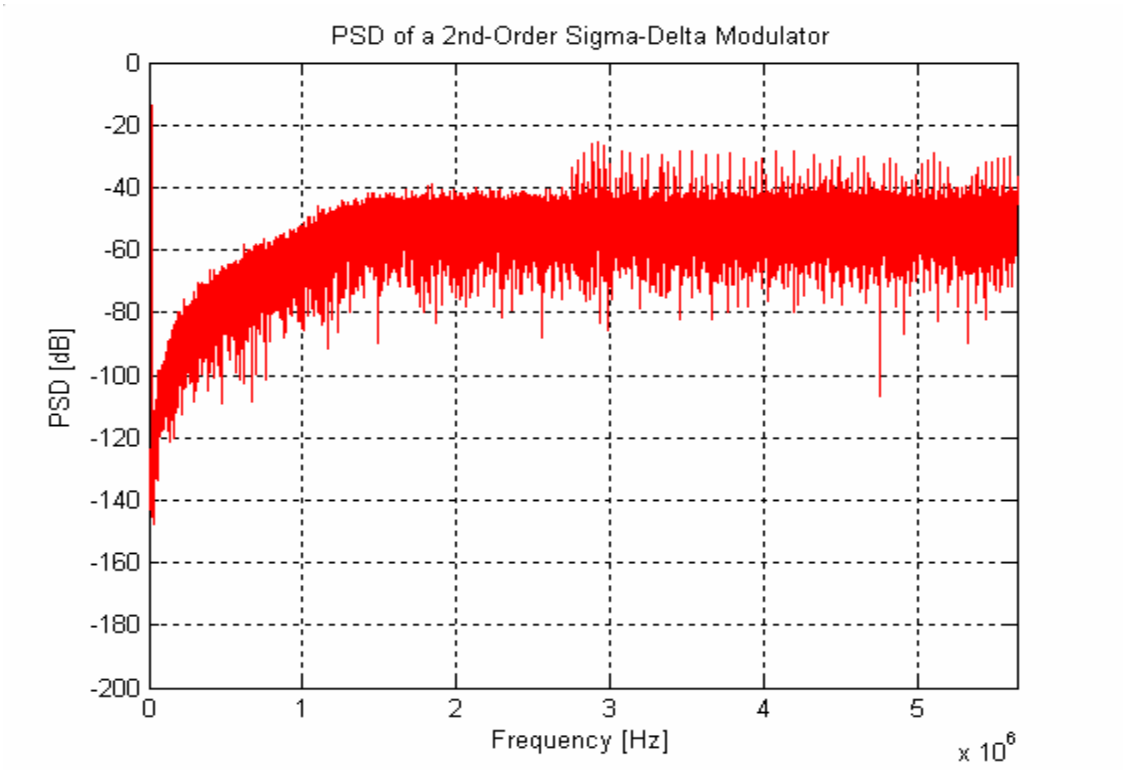


Figure 5: Power Spectral Density to 6 MHz on Linear Scale with OSR = 256.

Front End Architecture – Transistor Level

The front spice simulation has not been characterized in full, and thus a definite choice in architecture has not been chosen yet. However, what we most-likely will use is the architecture shown in Figure 6 below. The network consists of two digitized integrators, which each consist of a single operational transconductance amplifier with feedback capacitors for the integration operation. In addition to this a chopper is used on the front-end to help reduce offset errors between the input differential signals. The addition of buffers to the feedback loop will probably be implemented to cut down on the load that the comparator has to drive.

The clock generator remains to be built. We will need five total clocks; the main clock, two derivations that fit within the high and low phases, and these same two clocks delayed.

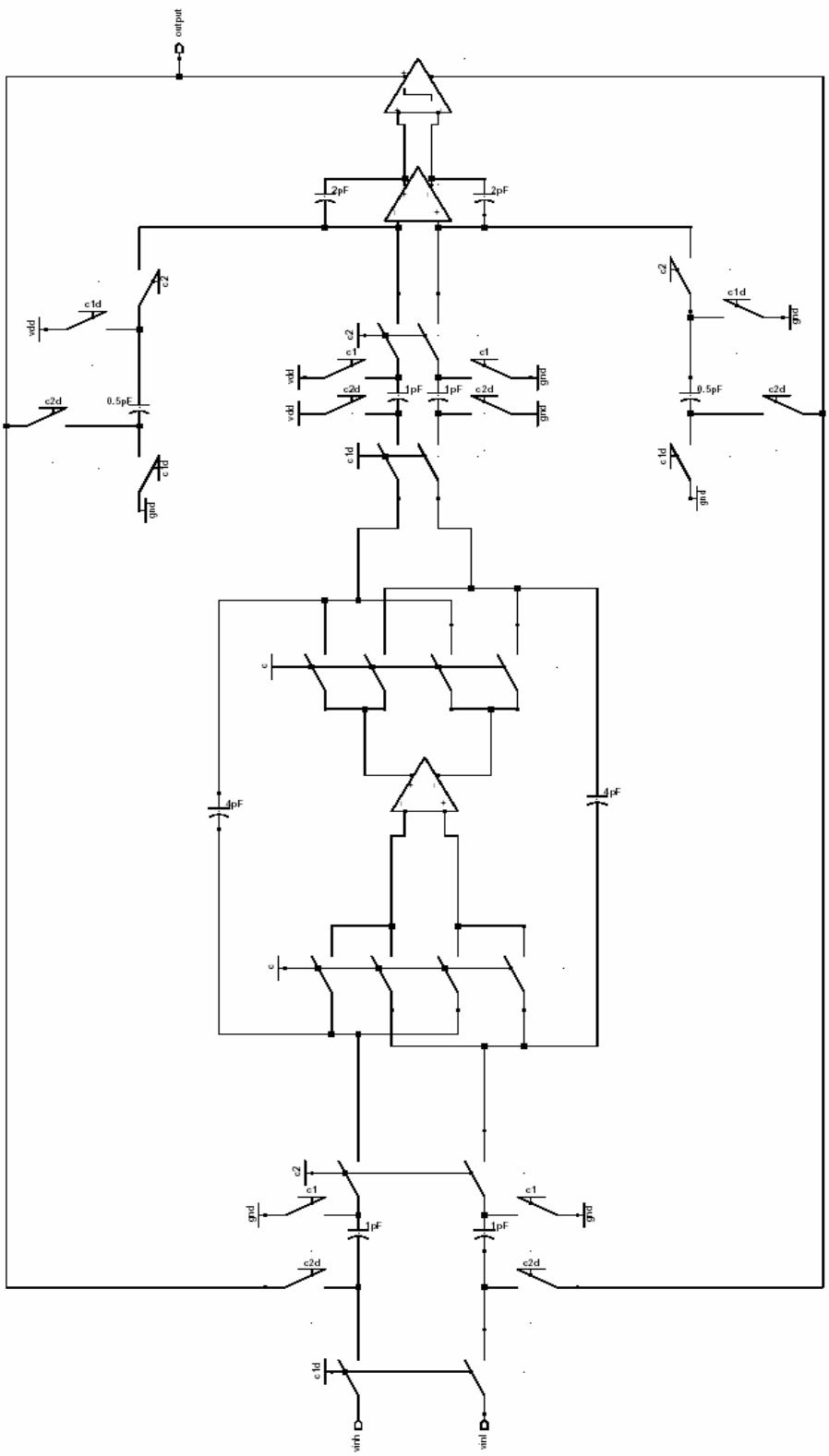


Figure 6: Architecture of second order front end. C is used to designate different clock signals

One of the main components of our design is an analog switch. A single transmission gate was found to be useful for all of the switches that need to be implemented. Initial sizing was carried out by calculating the charge time required on the capacitors, and extracting what resistance value would be needed to sufficiently charge them. HSPICE was used to do the characterization. The extracted resistance for this structure is 1.2 kohms, and the deviation of resistance throughout the IV curve is less than 5%. This indicates a worst case time constant of 2.4 ns for charging a 2pF capacitor. For the minimum charging time, this will produce an error of approximately 0.003 %, which is more than acceptable for the system we are building.

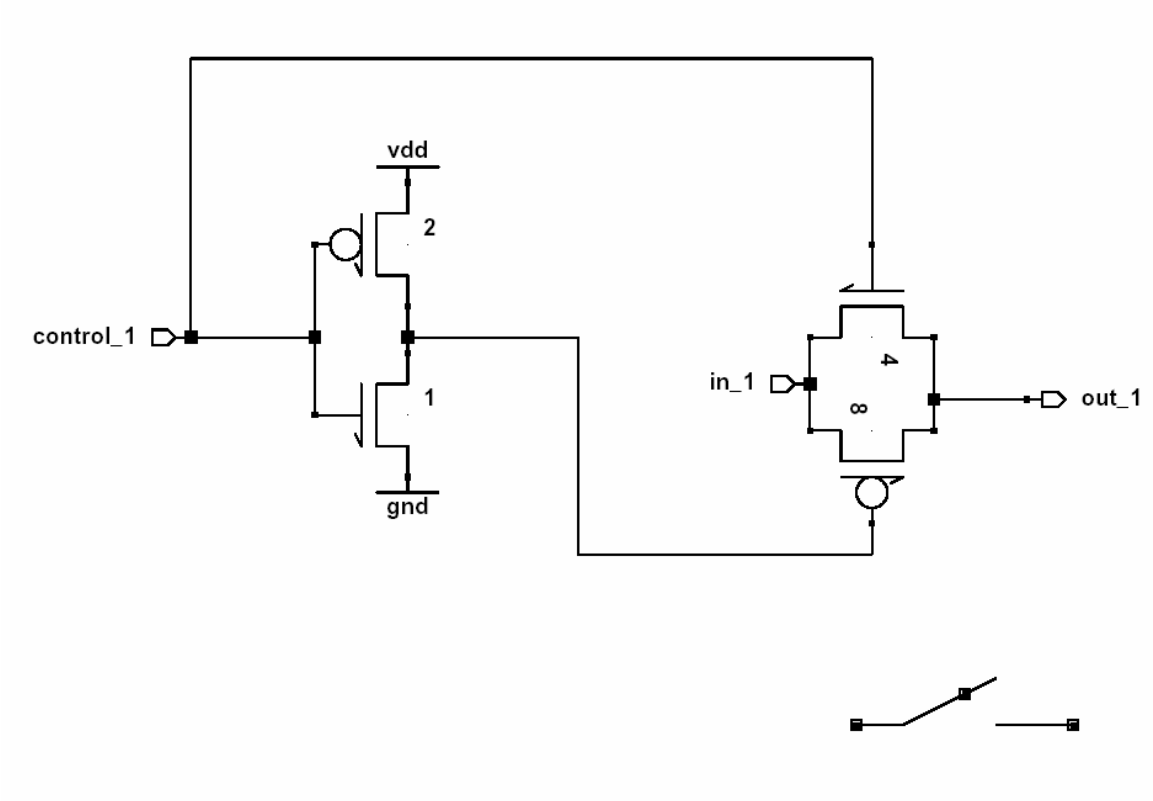


Figure 7: Transmission Gate

Operational Transconductance Amplifier (OTA)

The OTA is derived from a general design, and is pictured below. It consists of a differential amplifier driving a cascade load. This particular design implements a switched capacitor feedback circuit to ensure that the output signal remains close to Vdd/2. Two clocks, c1, and c2, are needed to implement the feedback loop. This will be done two of the clocks that are developed for the front end. The differential swing was found to be 3.9 V, and the transconductance is approximately 5.2 mA/V. The typical power dissipation was found to be just under 10 mw.

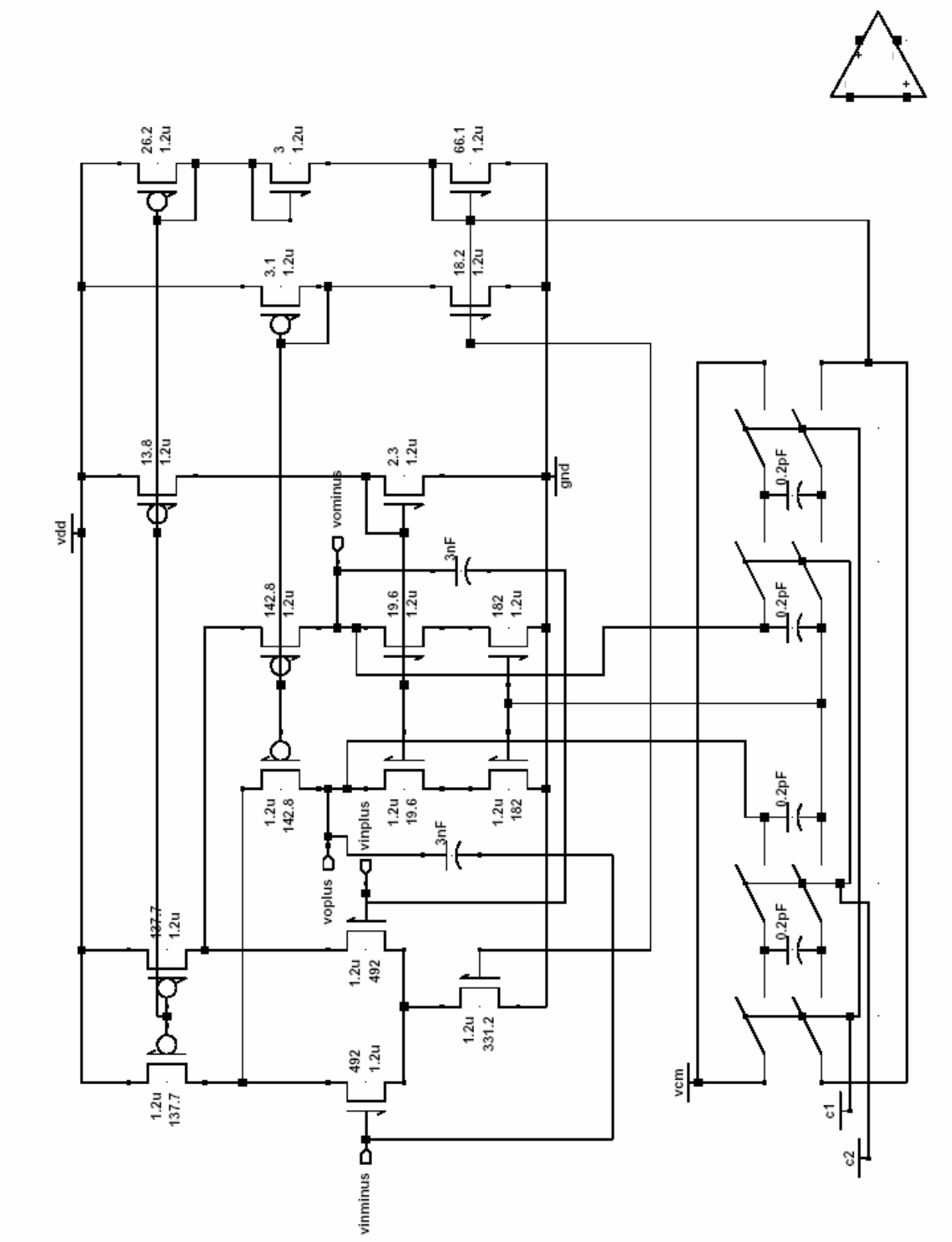
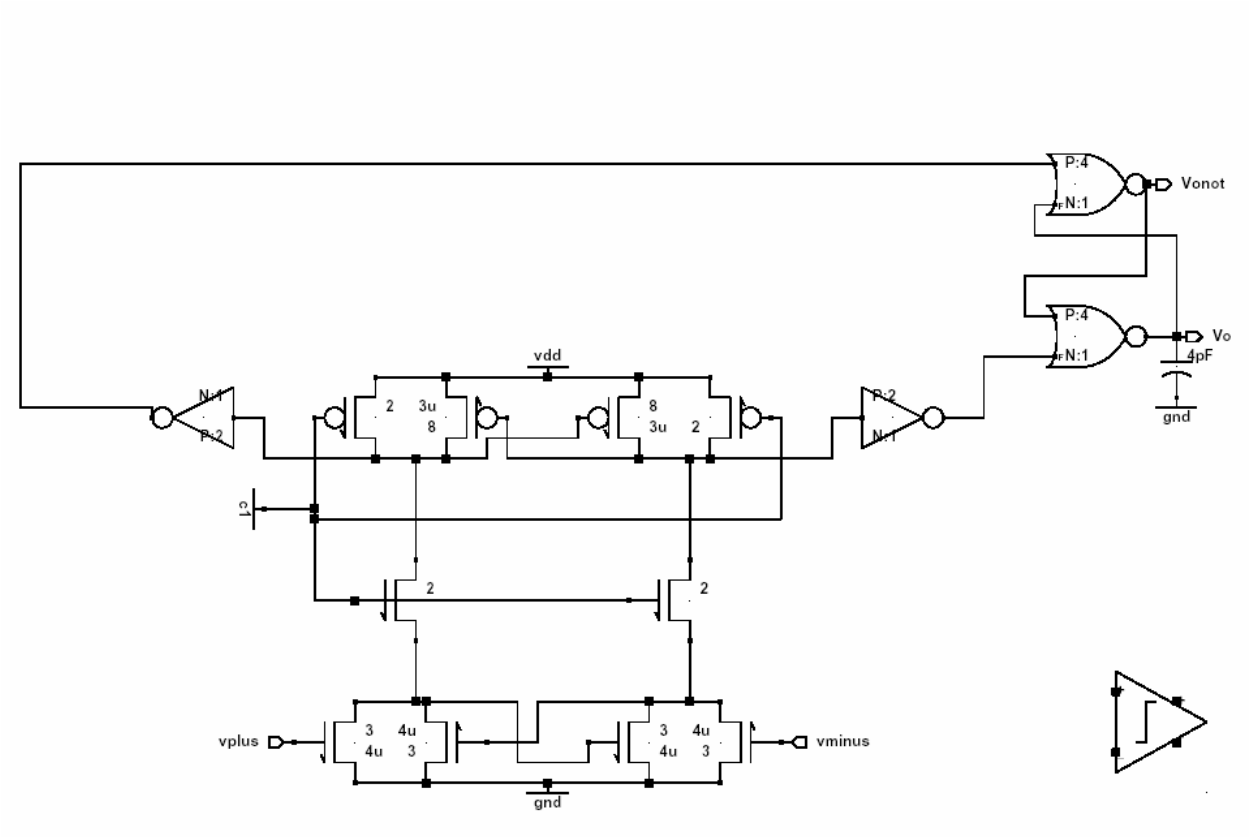


Figure 8: Operational Transconductance Amplifier

Comparator

The clocked comparator is implemented with a general regenerative latch that drives an SR flip-flop. The output is characterized with HSPICE, and a 4pF load is assumed. The slew rate is 100V/μs with this load. The maximum power, assuming constant switching for this circuit, was found to be 3.5 mw. The comparator voltage resolution is approximately 19 mv.



Time Audit

A large amount of time and effort was expended in getting the various tool flows going correctly. There were many issues with the AMI native technology that coupled with the MMI tool suite in unexpected ways. Essentially, the AMI tech went against a lot of the assumptions that had been made in creating the MMI tool set. Further, there have been some changes to the Calibre tool set as well, which needed to be accommodated. Finally, time was spent on getting cell characterization and library creation working. In passing, it should be noted that this has resulted in a bunch of user-friendly (!) scripts that the class could use.

Unfortunately, this means that not much time was left to work on the project itself! As it stands, for the back end, we have Simulink models for the sinc decimator stage that are working. These have been tested with a model for the second-order analog front end. Exploratory half band designs look promising, with as few as 9 distinct co-efficents for a 2:1 filter with cut-off starting at the signal band edge. In particular, these are in Canonical Signed Digit form, and entail only 124 additions.

Conclusion/ Direction

Front End

The front end architecture still needs to be simulated, and verified. The verification will take place against the Simulink model in the form of bit stream comparisons. In addition the front end needs to be layed out.

Back End

The sinc filter is easily implemented using counters/adders. For the later low-pass filters, we need a RAM/reg file for storing intermediate sample values. Further, we can use either a full-custom control logic with the CSD co-efficients embedded in the control flow or a ROM based control with stored co-efficients. Currently, we plan on going with a ROM based design as that will accommodate design changes easier. Both the RAM and the ROM are to be designed using the MegaCell compiler from MMI. A working 0.25u SRAM MegaCell is included in the distribution – the plan is to adapt this to our technology for the final design. The ROM will be a NOR design a la the final exam.

References

[1] T. Saramaki, "Design of FIR filters as a tapped cascaded interconnection of identical subfilters", IEEE Trans. On Circuits and Systems, vol. 34, pp1011-1029, Sept. 1987.
[2] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto and F. Maloberti", Modeling Sigma-Delta Modulator Non-Idealities in SIMULINK", *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS '99)*, 2, Orlando, USA, pp. 384-387, 1999.