ECE 224a -- Syllabus
Forrest Brewer

ECE 224a is a VLSI project lab in which students construct designs which are submitted to MOSIS and subsequently tested. The course is “advanced” in that at least 1 prior VLSI class is required, and 2 are preferable. The onus is not in the teaching of tools, but in design construction within a practical flow.

Topics:
Layout/Fabrication
- Device Layout: contact, resistor, cap, transistor
- Cell Layout: std. cell constraints, abstraction, LEF/DEF, scaling
- Block Layout: Floorplanning and WirePlanning
- Clock and Power Layout

VLSI Devices: MOS Transistors, Caps, Diodes, etc.
- Device Variability: (sea of devices and moment reduction)
- High Voltage: ESD, Driver, Guard Rings, Noise Mitigation, Rad Hardness

Analysis
- Transient (Spice, coupling, noise modeling, jitter)
- Logical (Verilog, Static Timing, Power Analysis)
- Transaction Level (C, system-C, Bluespec)

Data-Path and Memory Circuits
- Static/Dynamic Memories
- Ancillary Memory Analog Circuits

Analog Layout
- Noise Issues: Substrate, Coupling, Power
- Variability and Matching
- Analog Device Layout