Designing Sequential Logic Circuits

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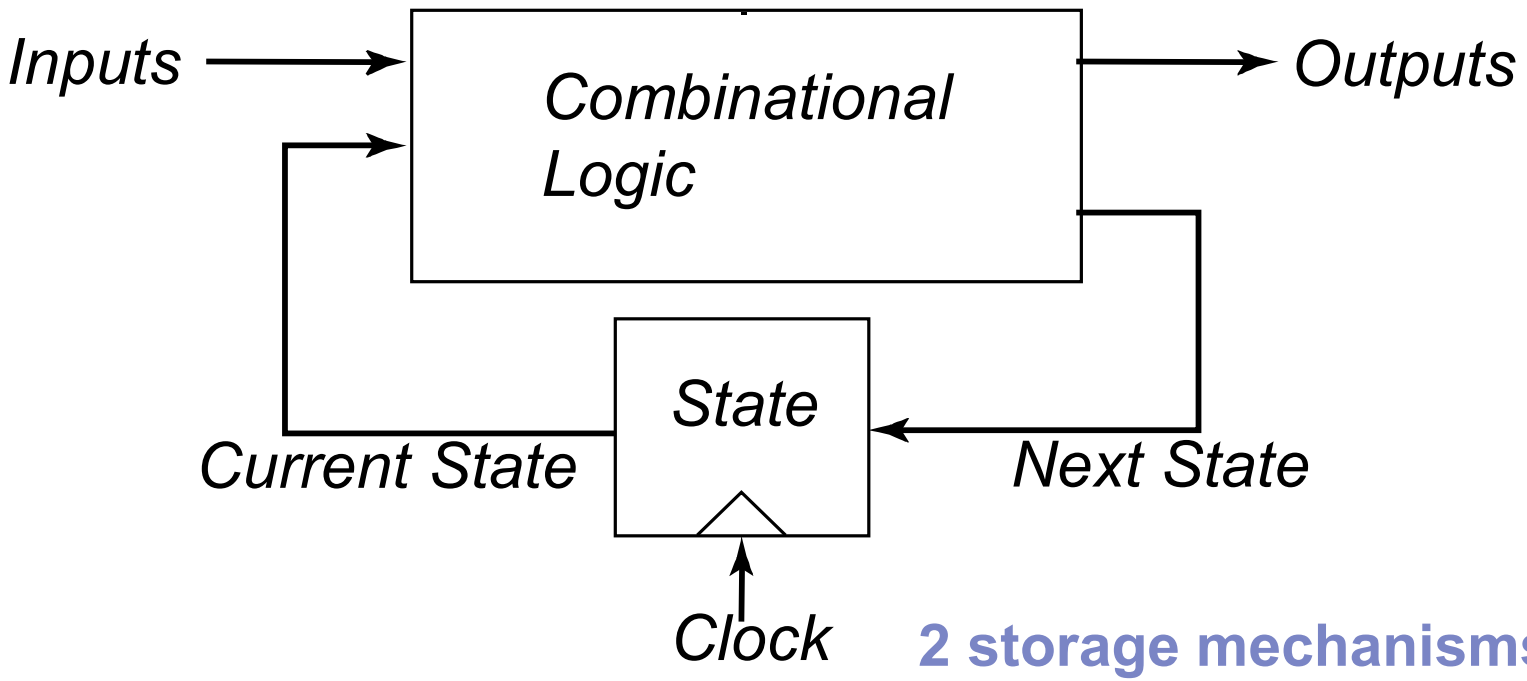
Sequential Logic



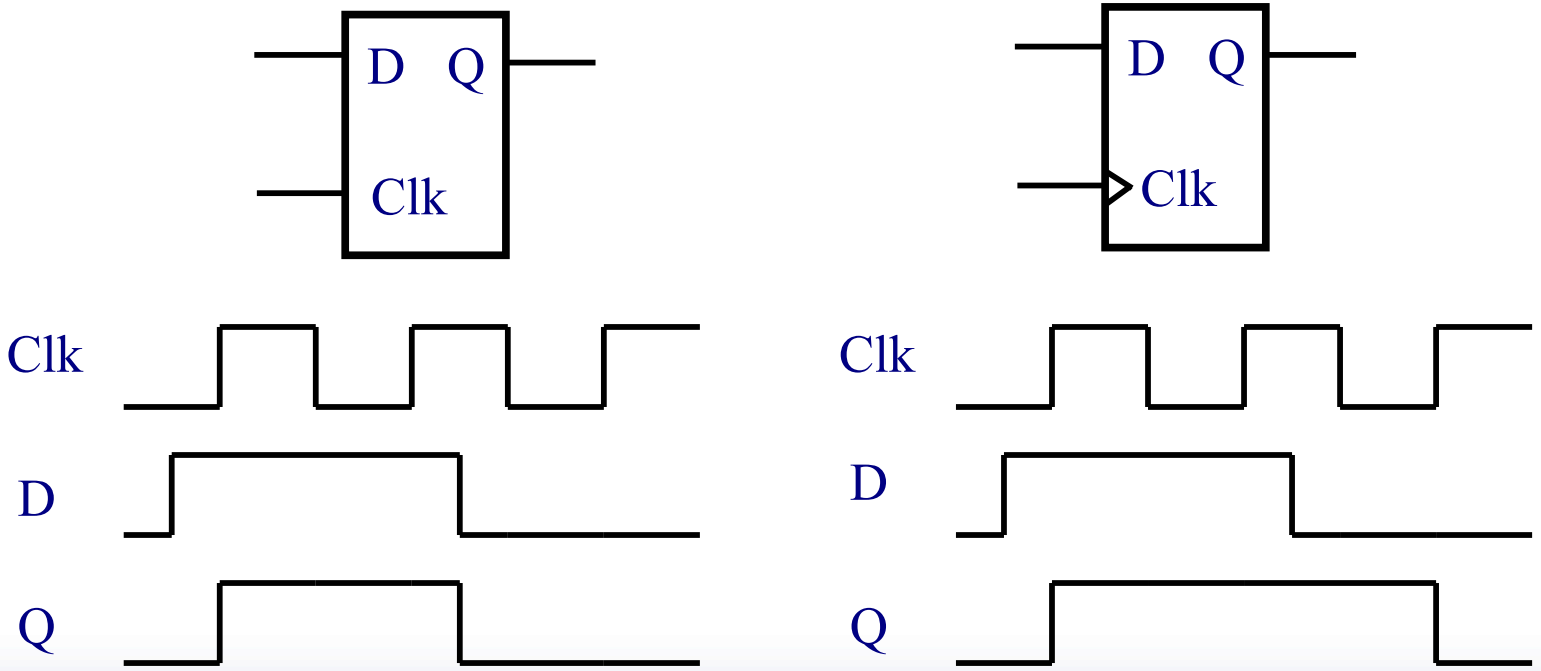
2 storage mechanisms:
- **positive feedback**
- **charge-based**

Naming Conventions

- In the text:
  - a latch is level sensitive
  - a register is edge-triggered
- Many different naming conventions:
  - flip-flops (level or edge?)
  - Transparency?
  - Dual edge/level

Latch versus Register

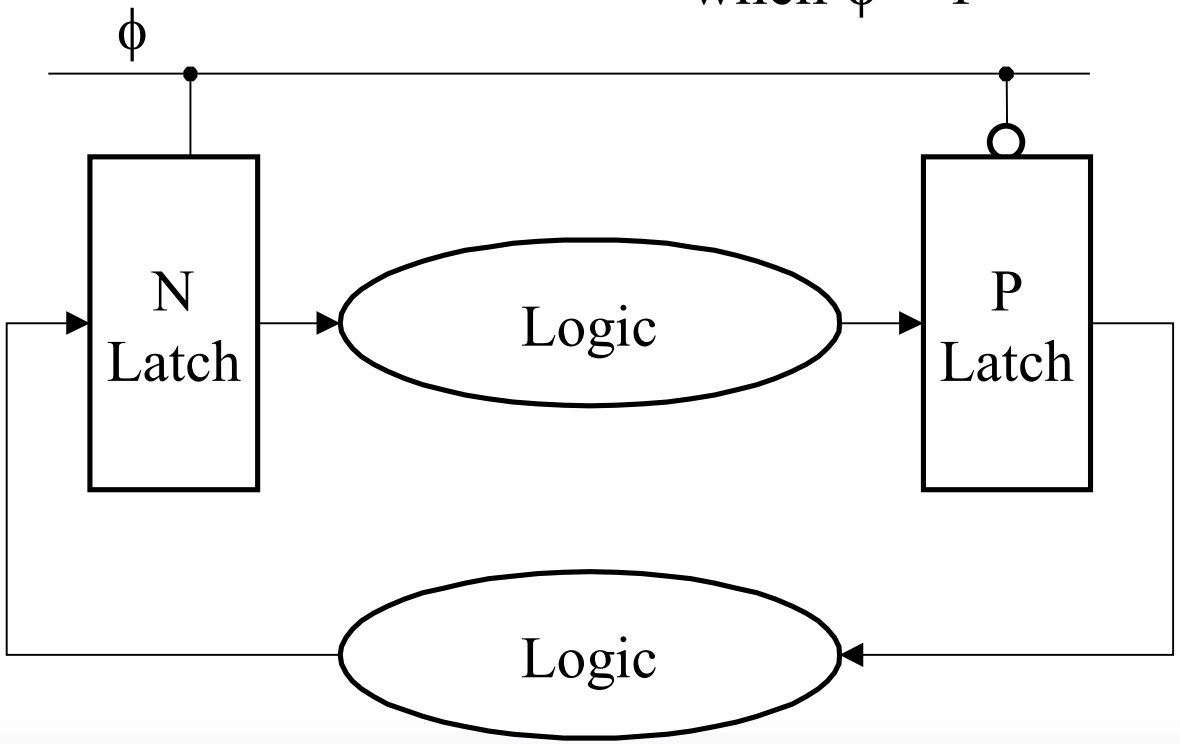
- Latch- stores if clock is low transparent if clock is high
- Register- stores if clock rises, never transparent (mostly)



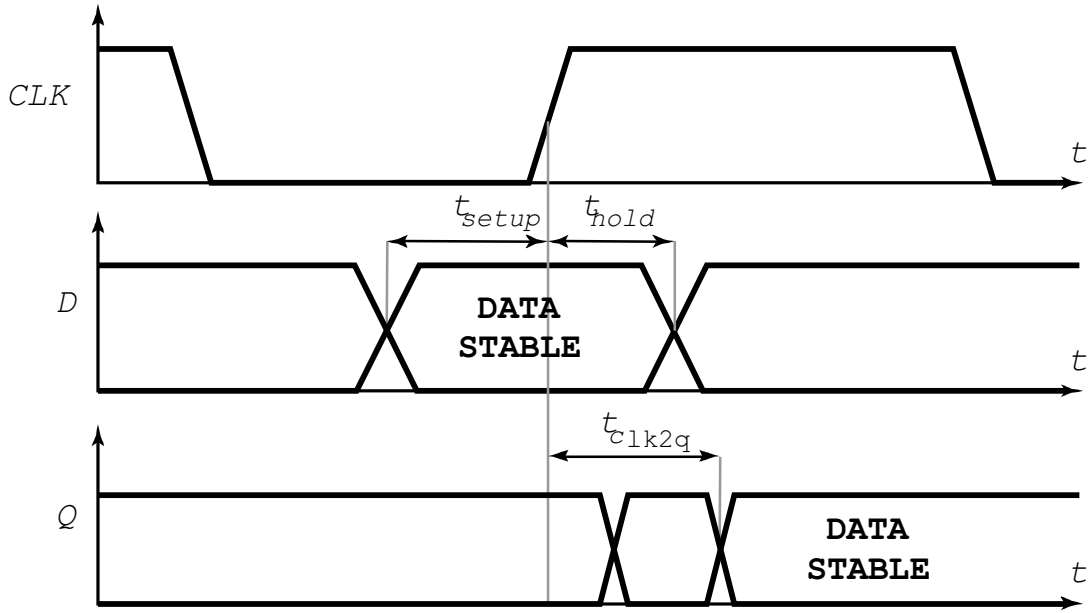
Latch-Based Design

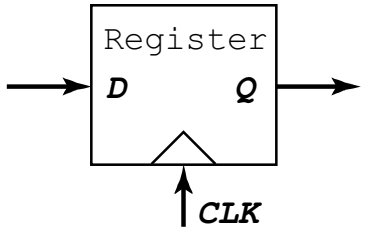
• N latch is transparent when $\phi = 0$

• P latch is transparent when $\phi = 1$

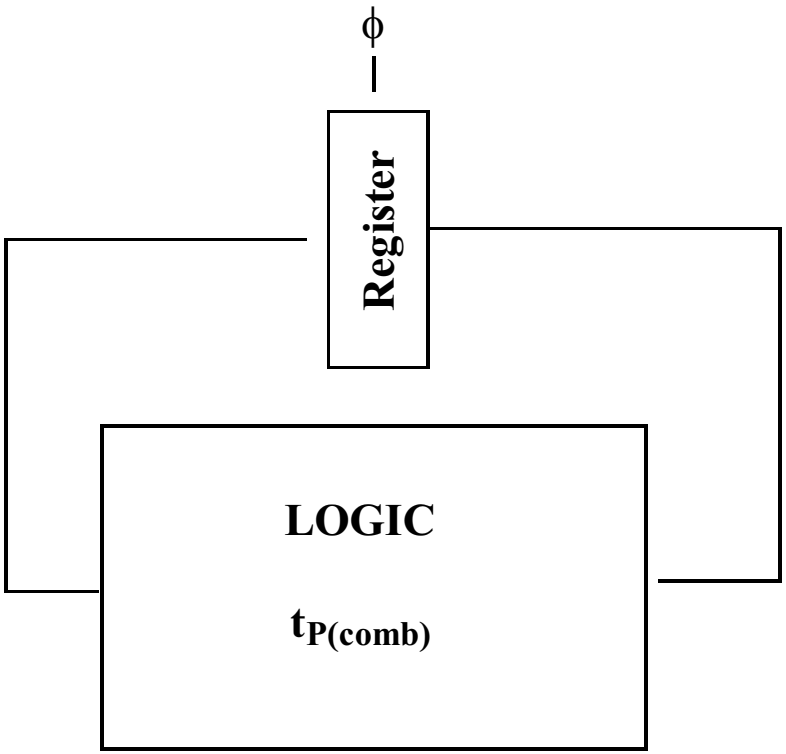


Timing Definitions





Maximum Clock Frequency



Timing Constraints:

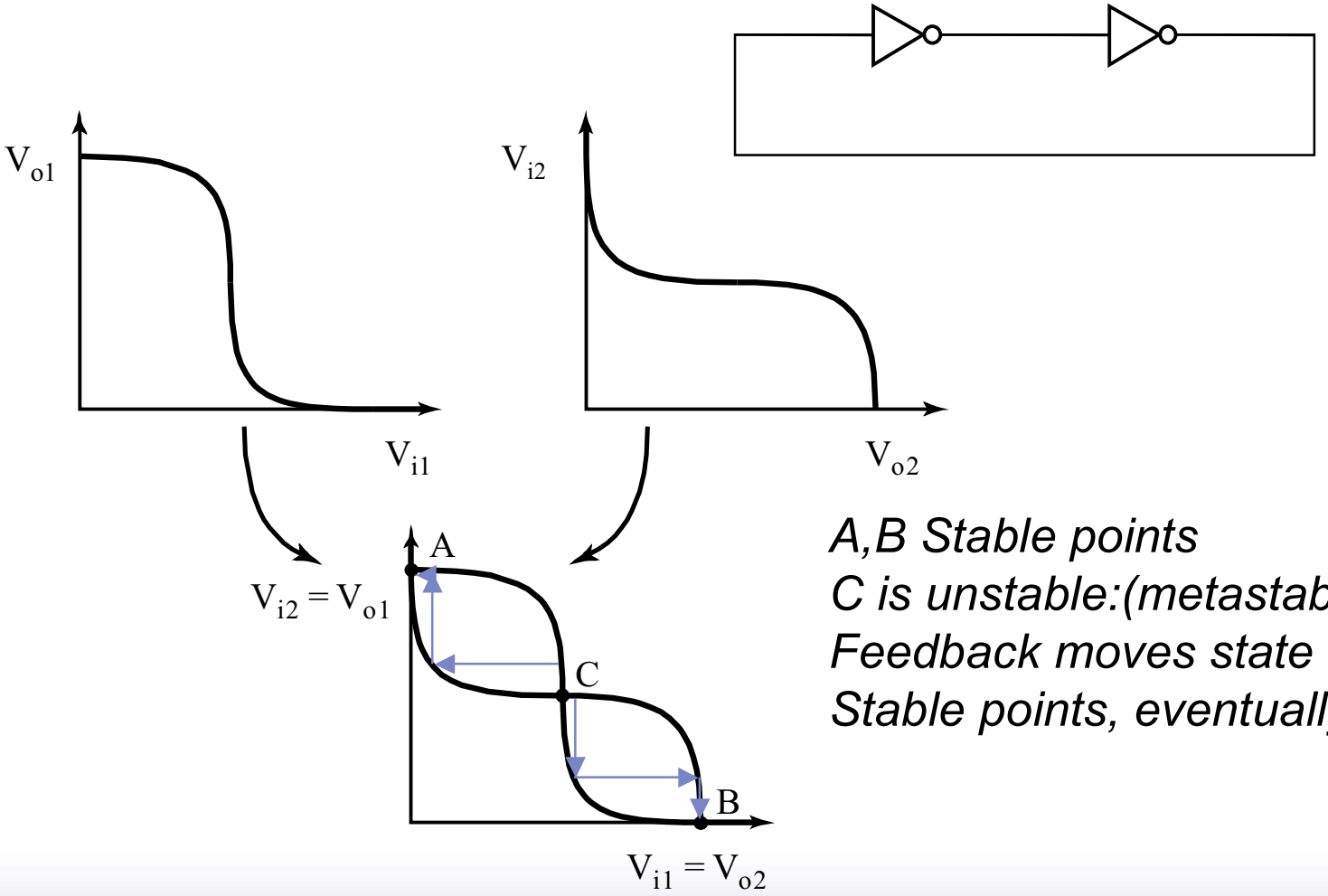
$$t_{clk2q} + t_{p(comb)} + t_{setup} = T$$

$$t_{cdreg} + t_{cdlogic} > t_{hold}$$

First Constraint ensures clock is slow enough that Registers sample correct value

Second Constraint ensures that there is no path after the clock changes to alter the previously stored data

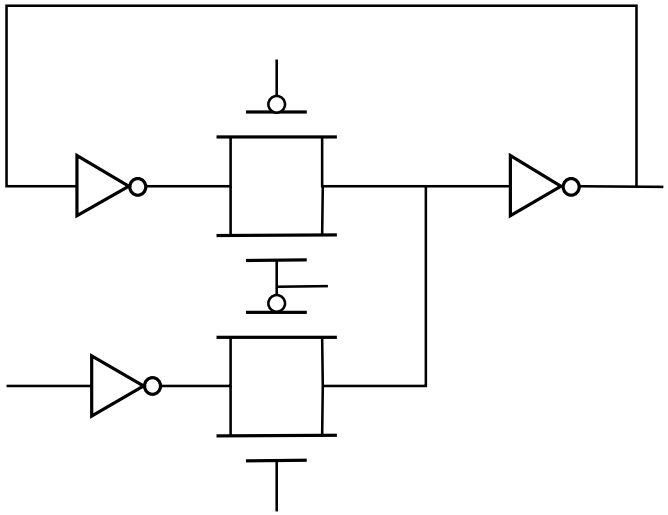
Positive Feedback: Bi-Stability



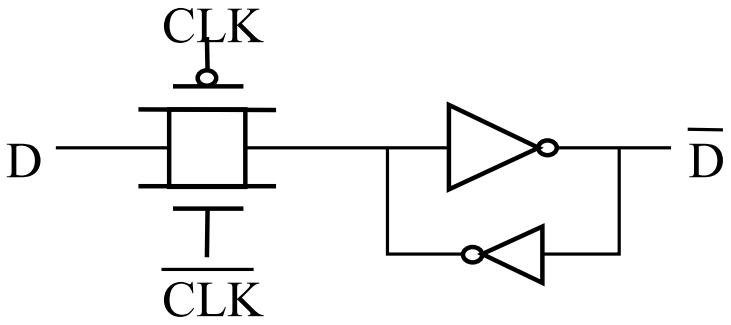
A,B Stable points
C is unstable:(metastable)
Feedback moves state to Stable points, eventually

Writing a Static Latch

Use the clock to distinguish between the transparent and opaque states



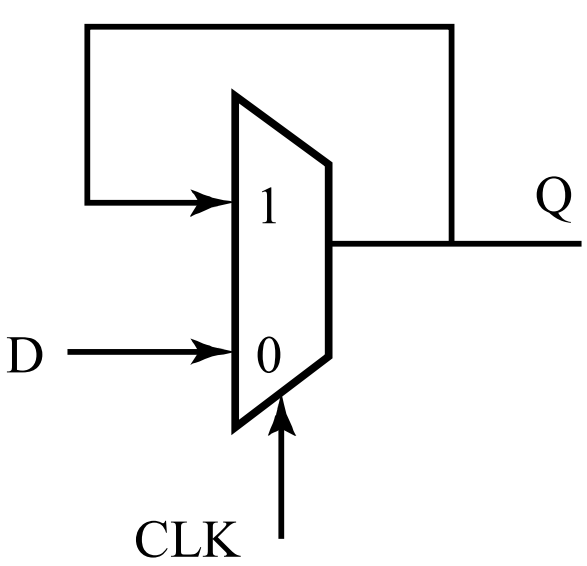
Converting into a MUX



Forcing the state
(can implement as NMOS-only)

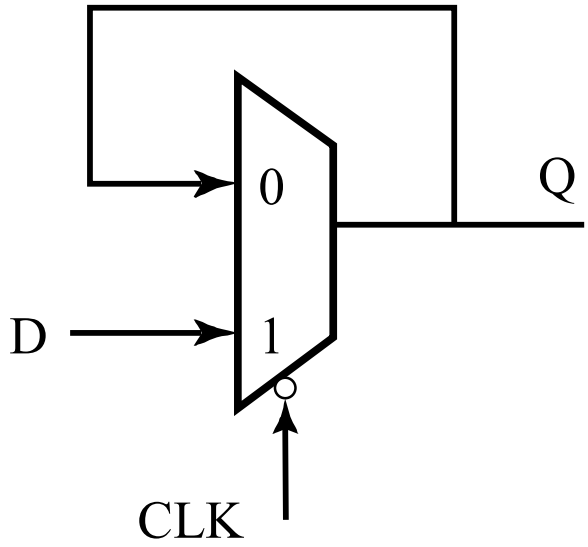
Mux-Based Latches

Negative latch
(transparent when CLK= 0)



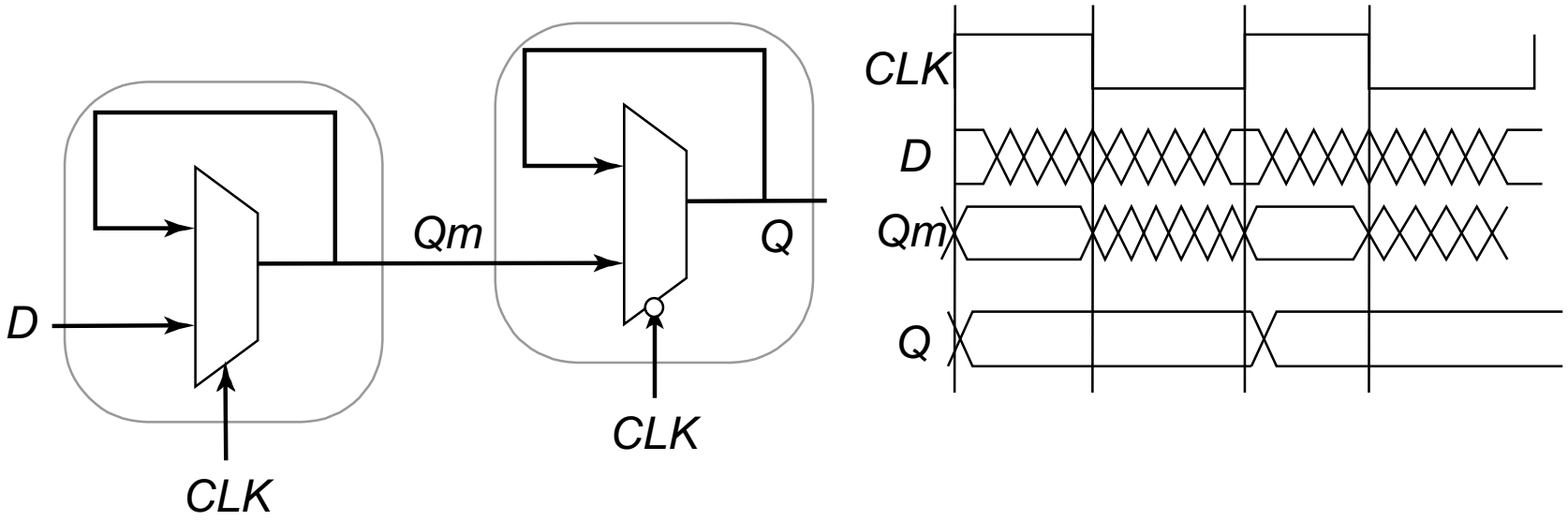
$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Positive latch
(transparent when CLK= 1)



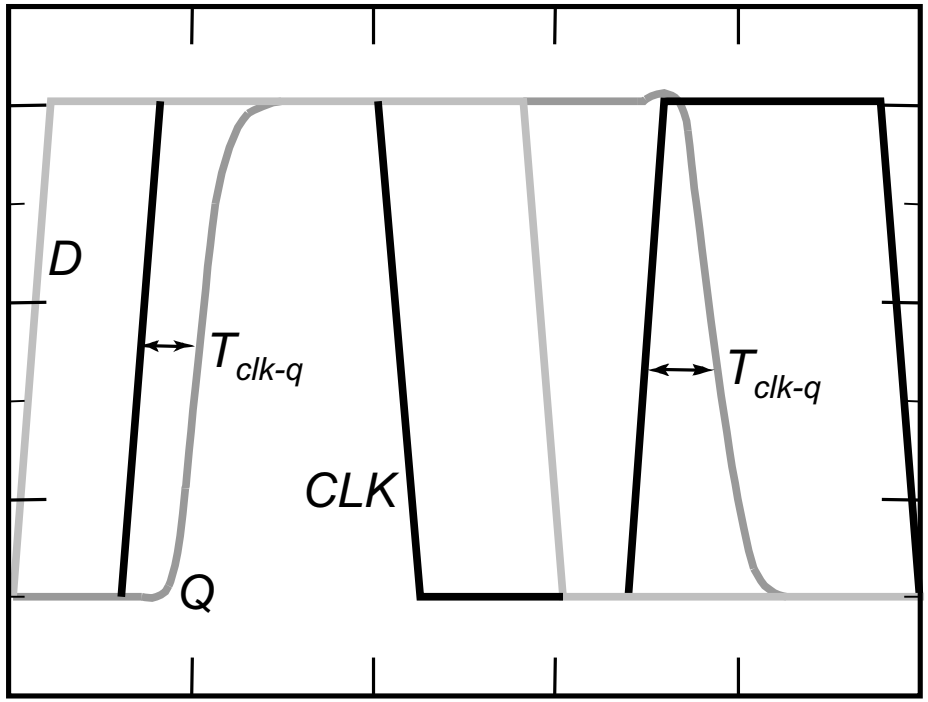
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

Master-Slave Register



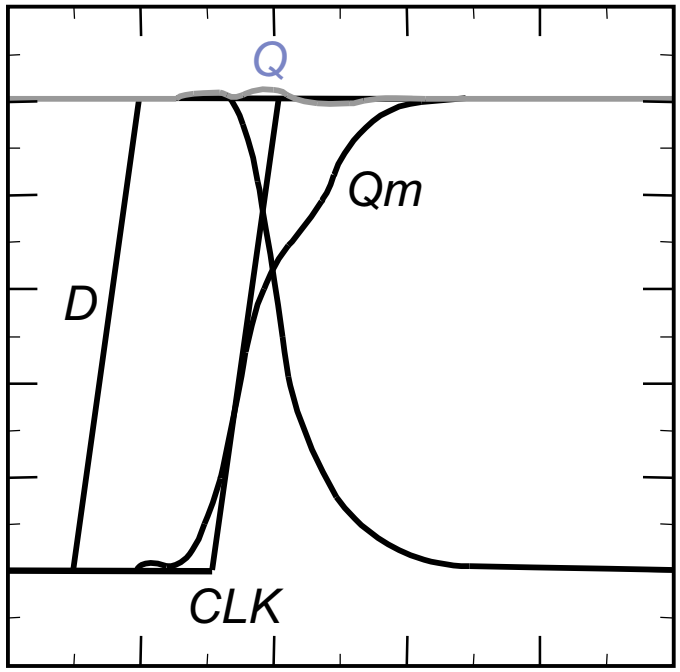
Two opposite latches trigger on edge
Also called master-slave latch pair

Clk-Q Delay

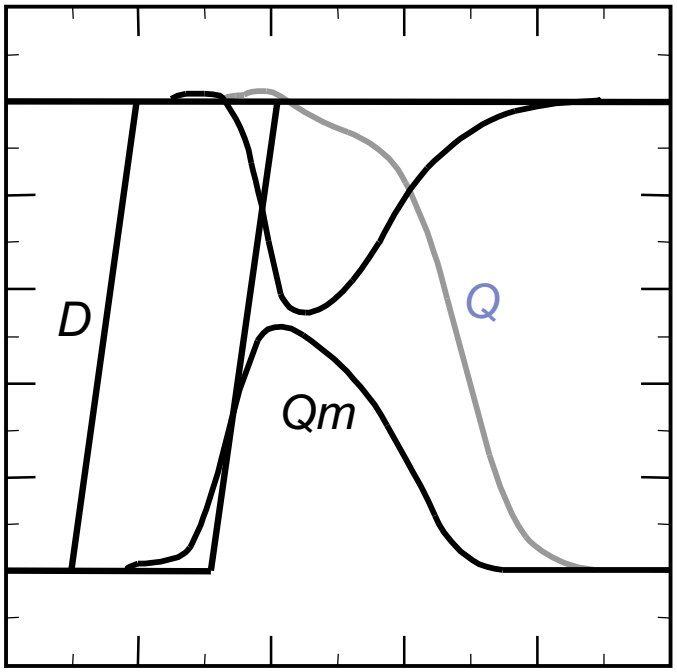


Clock to Q delays are
Different for rising and falling
Transitions
Use Worst Case – not Avg!

Setup Time (MS register)

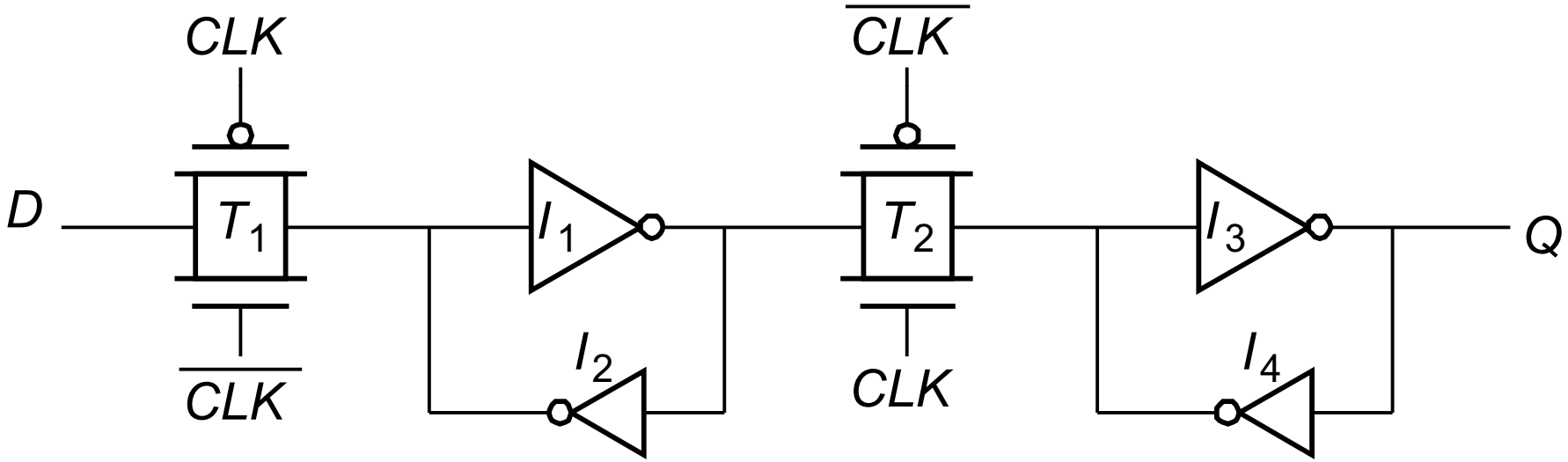


Setup = 0.21nS
Passed D



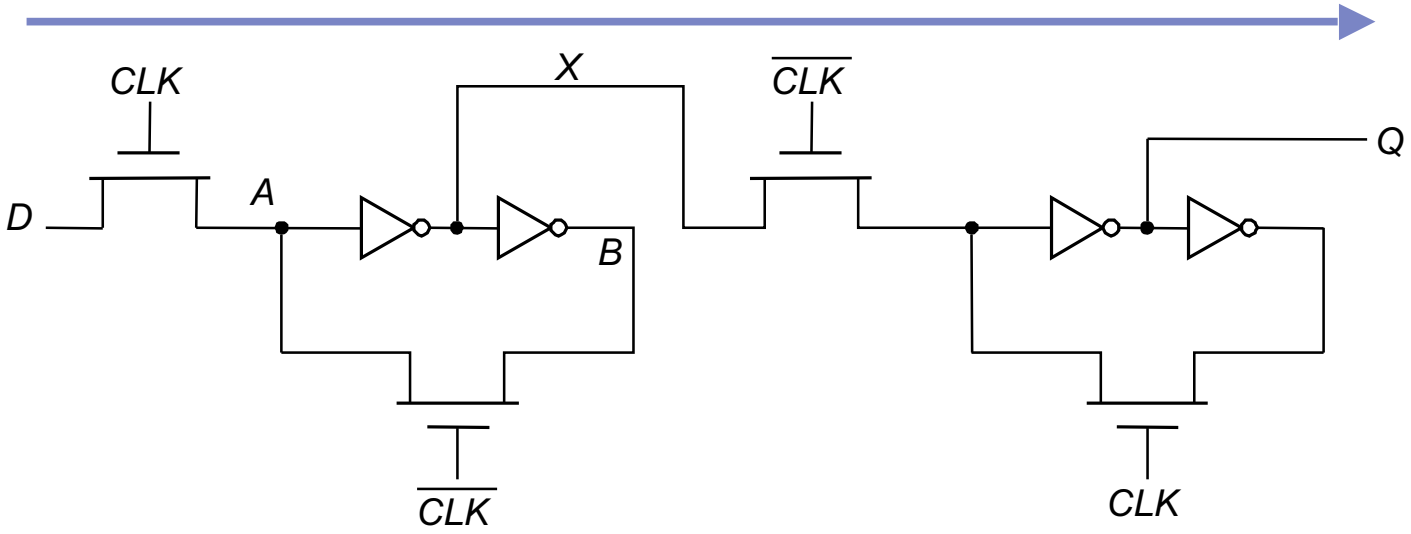
Setup = 0.20nS
Failed to pass D

(Pseudo Static) Master-Slave Register

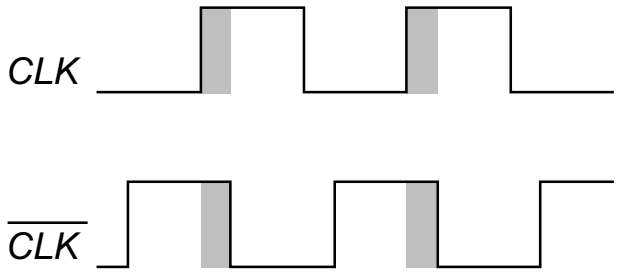


- *Reduced load on Clock*
- *Possible Backward flow of data*
  - *Reduce strength of I2 and I4*

Avoiding Clock Overlap



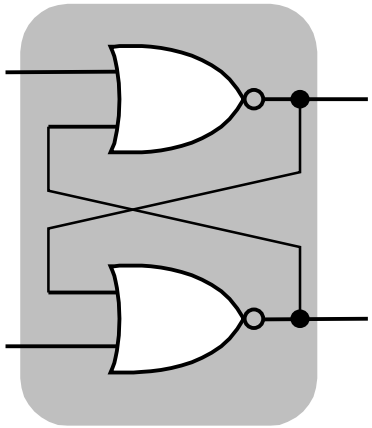
(a) Schematic diagram

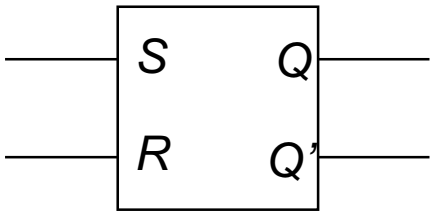


(b) Overlapping clock pairs

Cross-Coupled Pairs

NOR-based set-reset

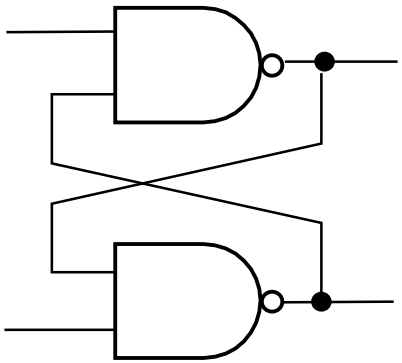




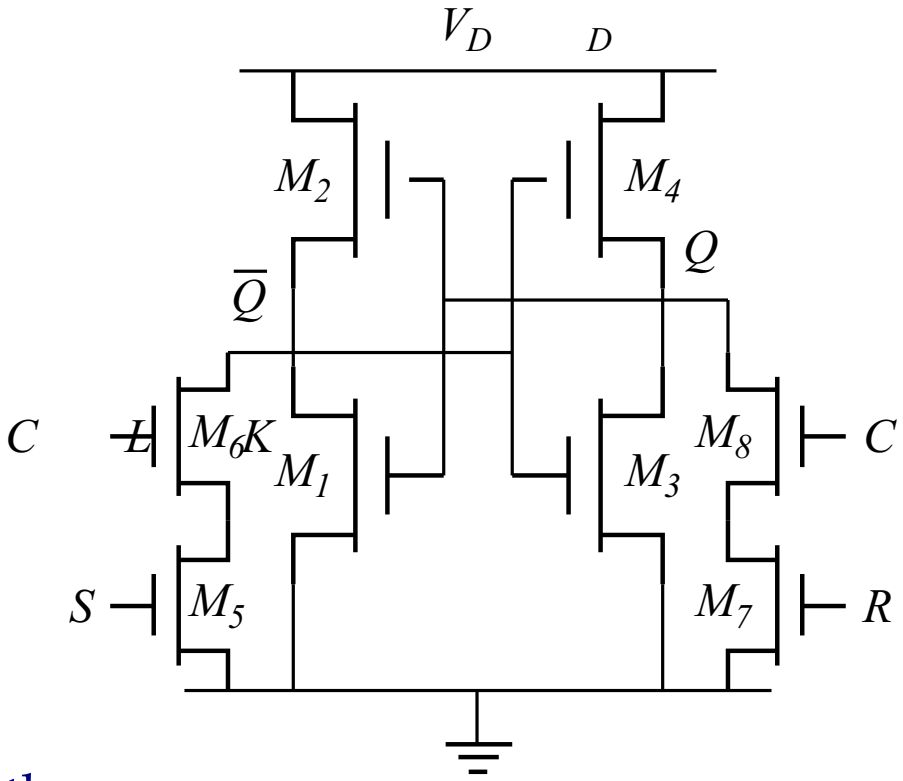
S	R	Q	Q'
0	0	Q	Q'
1	0	1	0
0	1	0	1
1	1	-	-

Cross-Coupled NAND

Cross-coupled NANDs

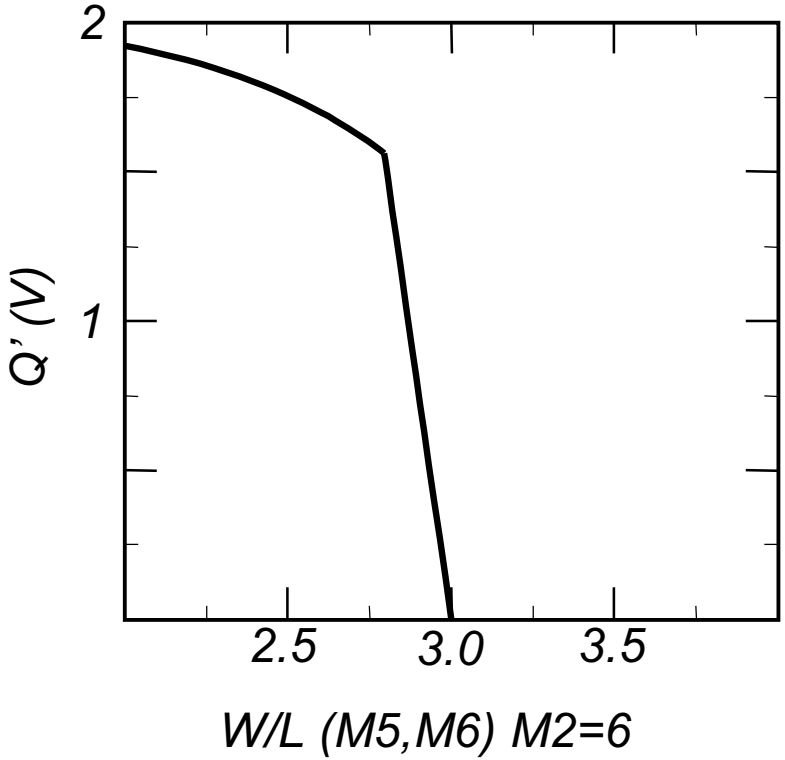


Added clock

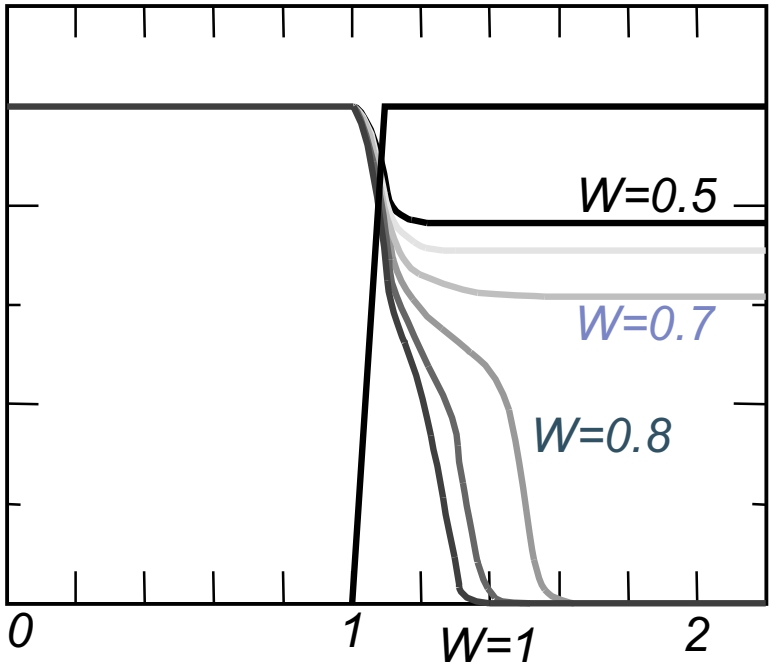


This is not used in datapaths any more, but is a basic register memory cell

Sizing Issues



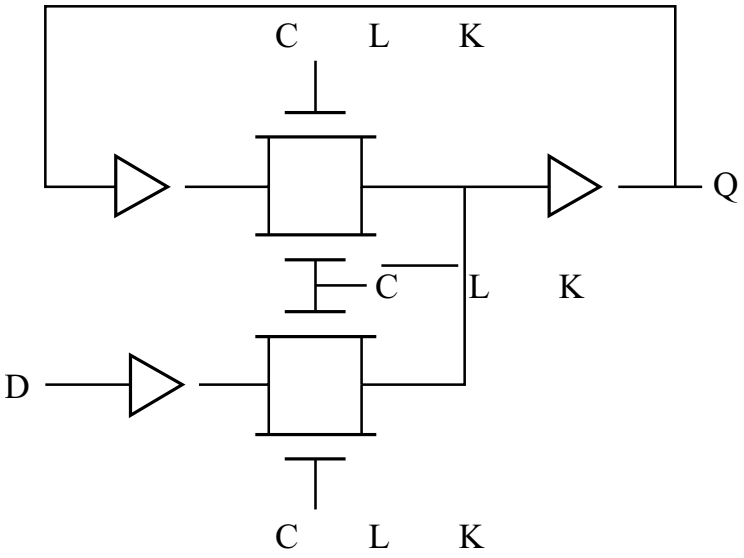
Output voltage dependence on transistor width



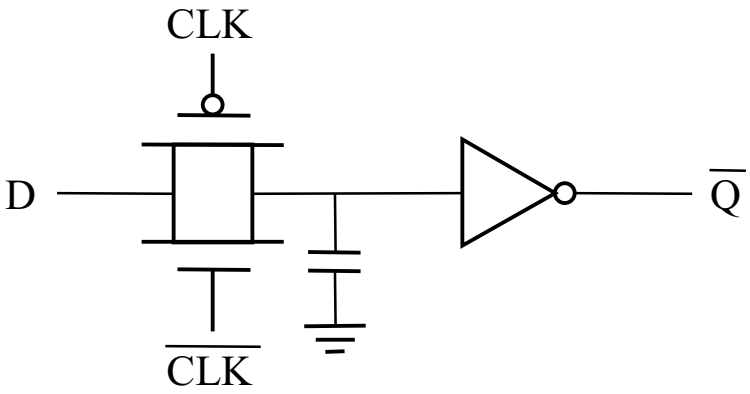
Transient response

Storage Mechanisms

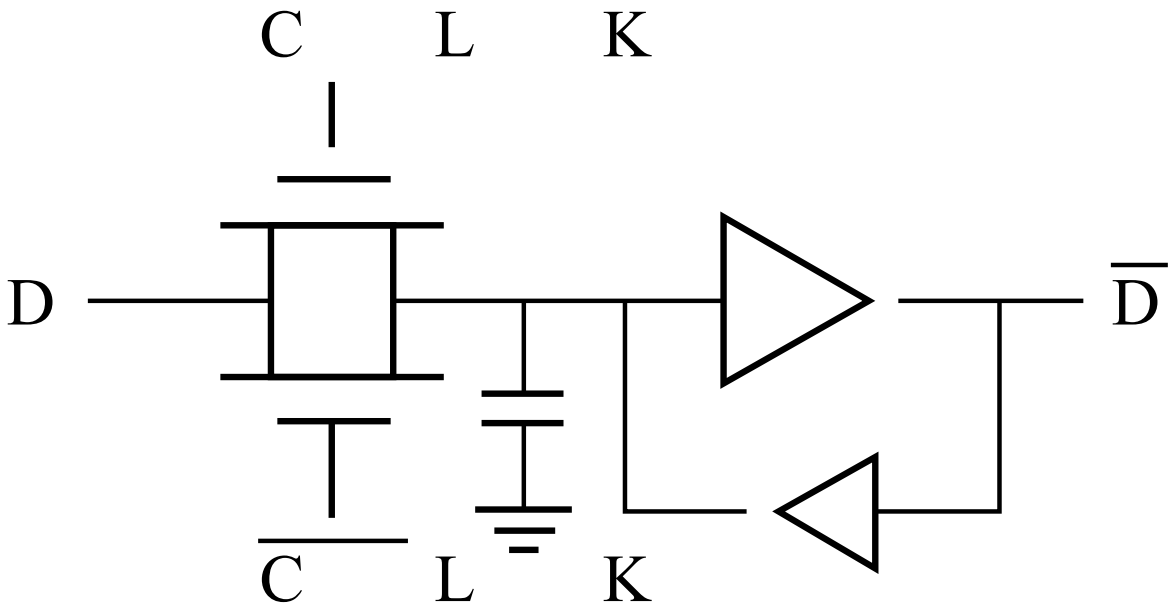
Static



Dynamic (charge-based)

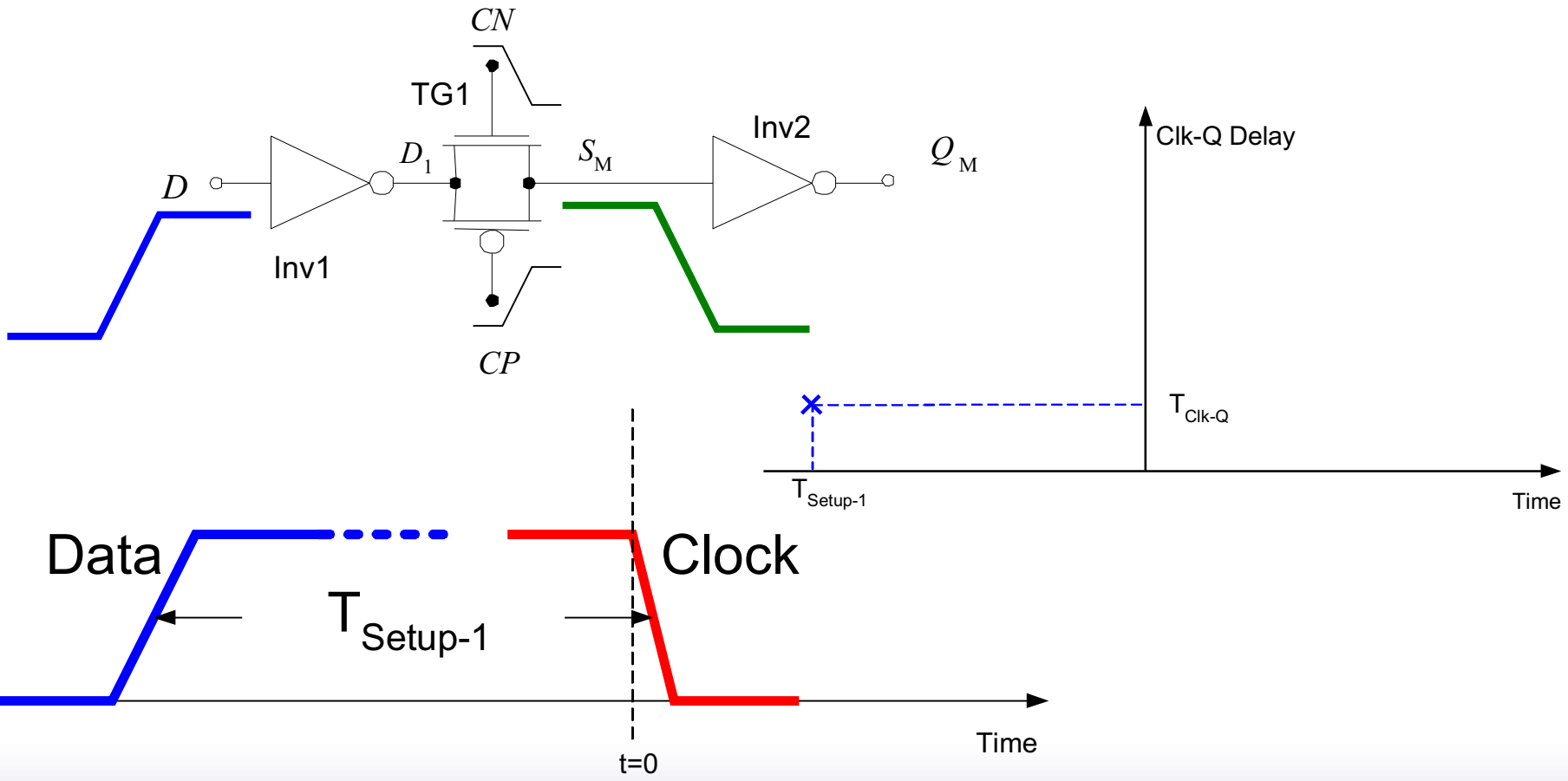


Making a Dynamic Latch Pseudo-Static



Setup/Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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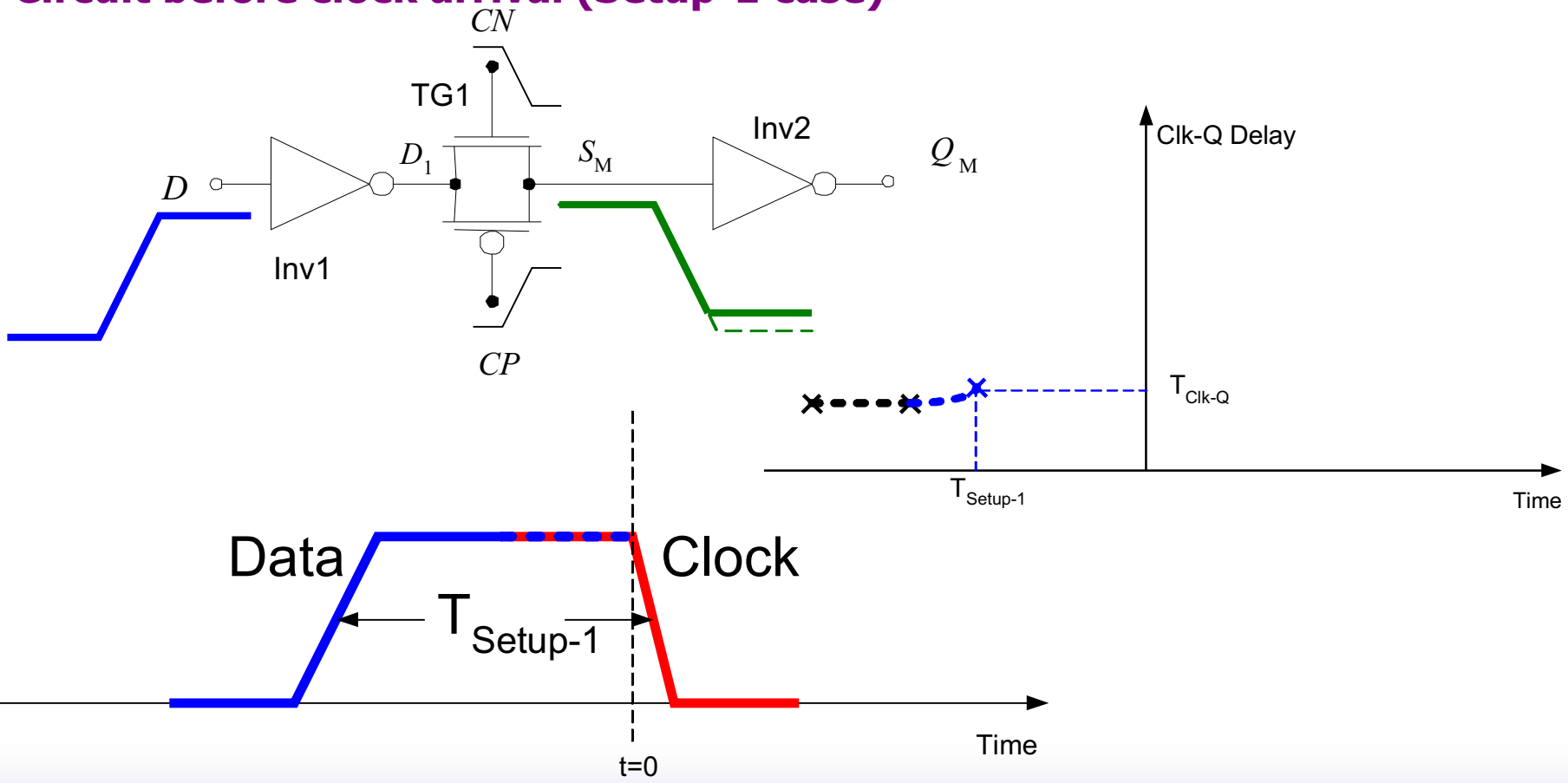

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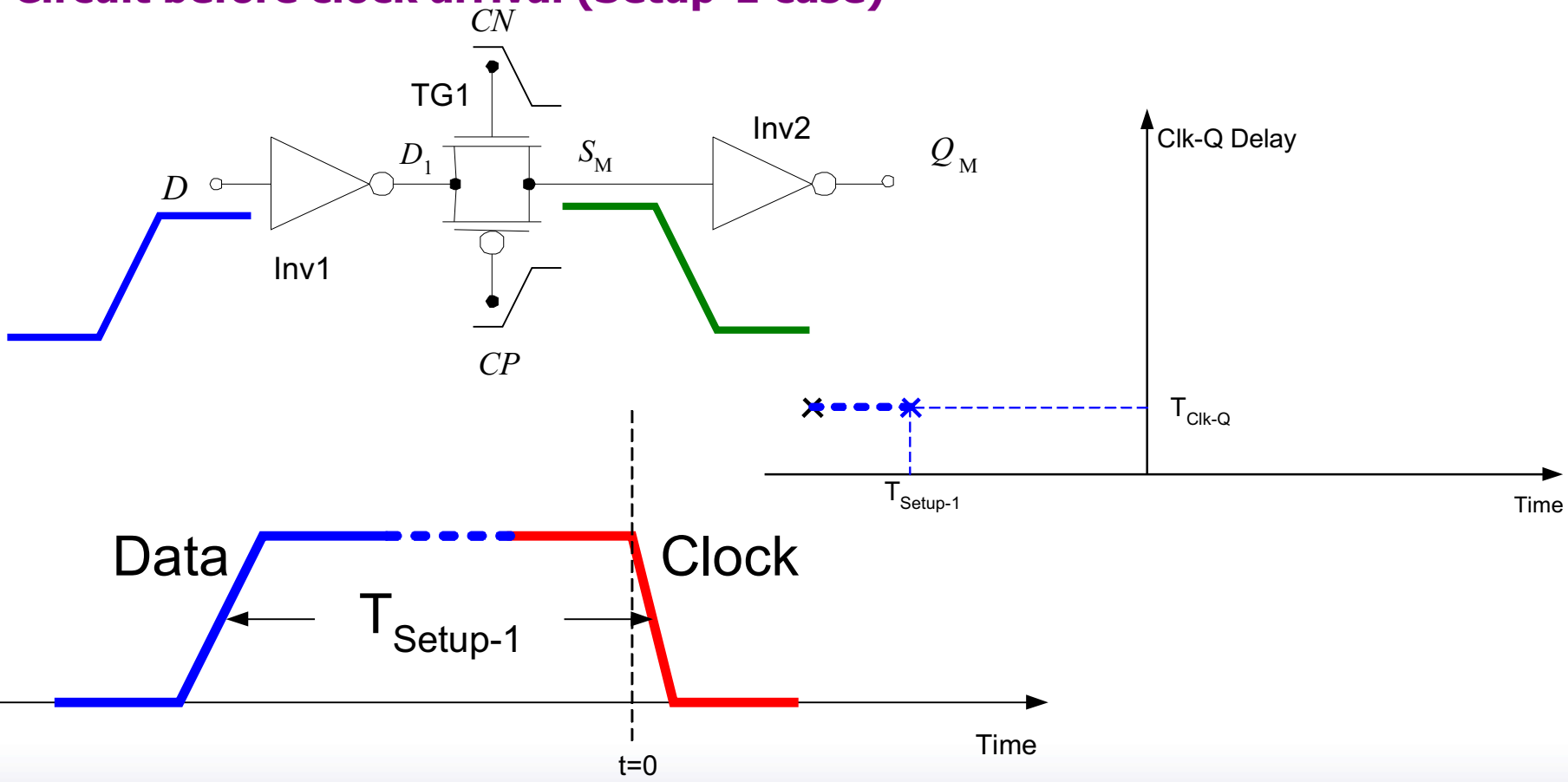
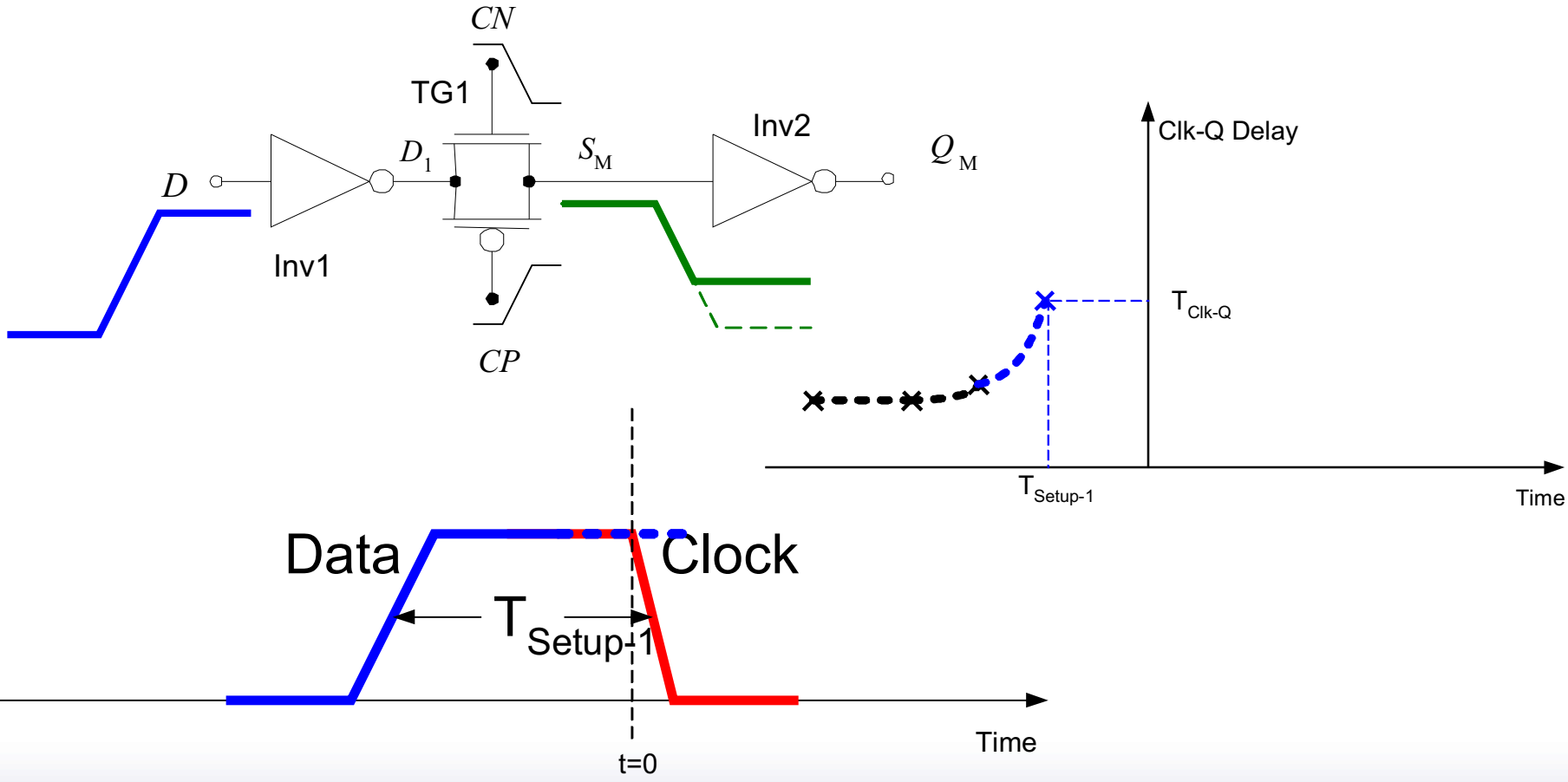
Circuit before clock arrival (Setup-1 case)



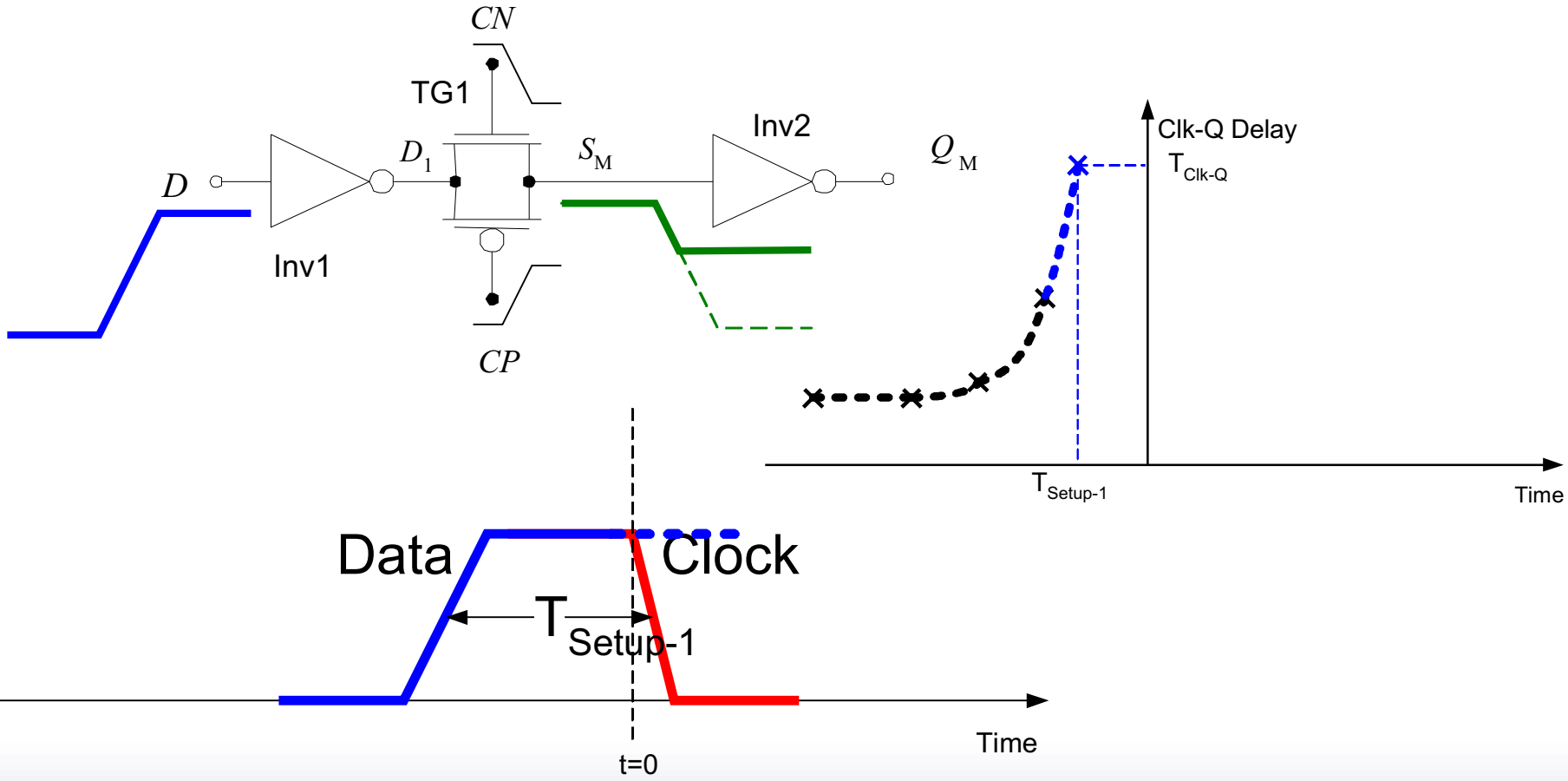
Setup/Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

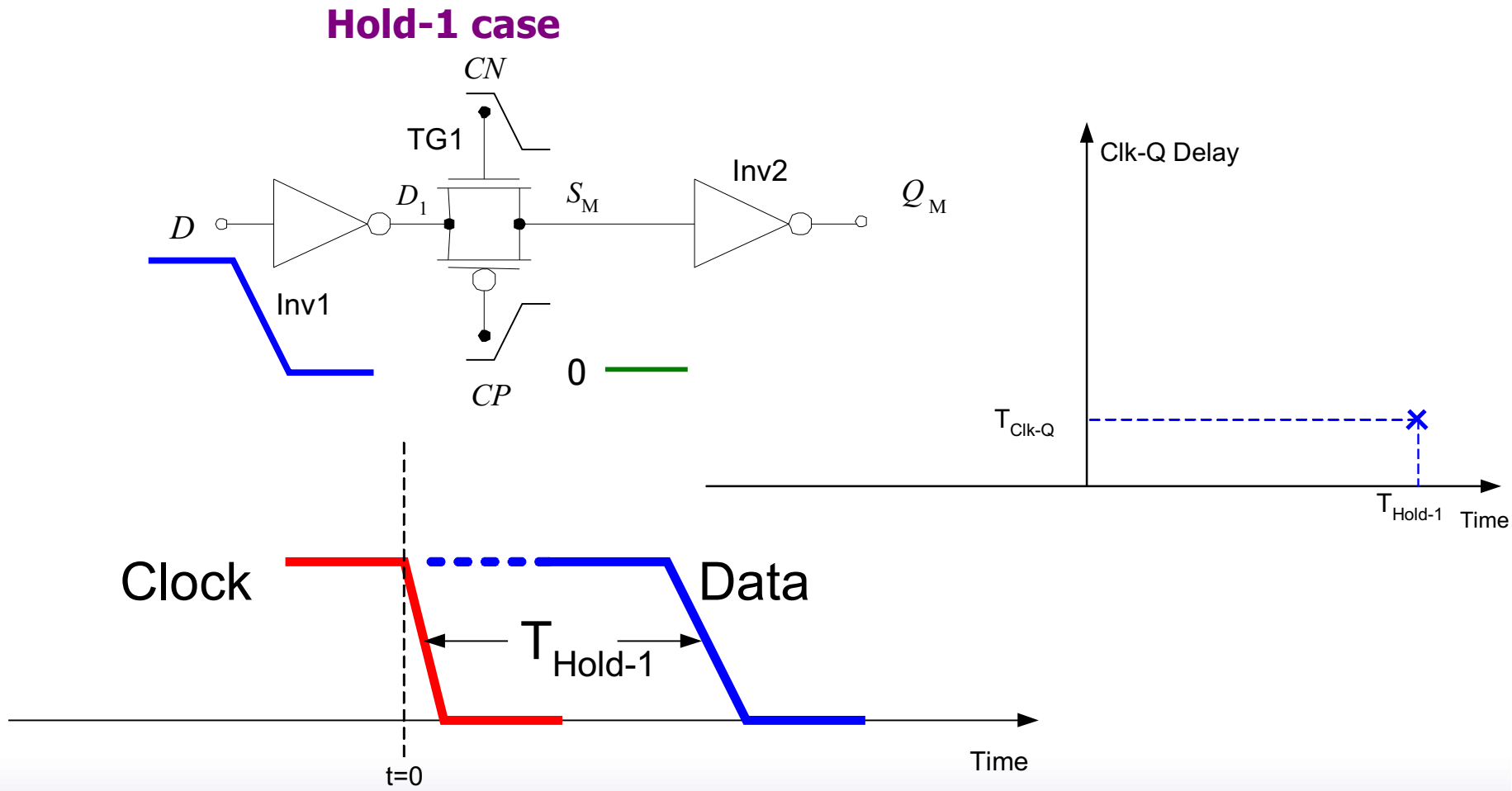


Setup/Hold Time Illustrations

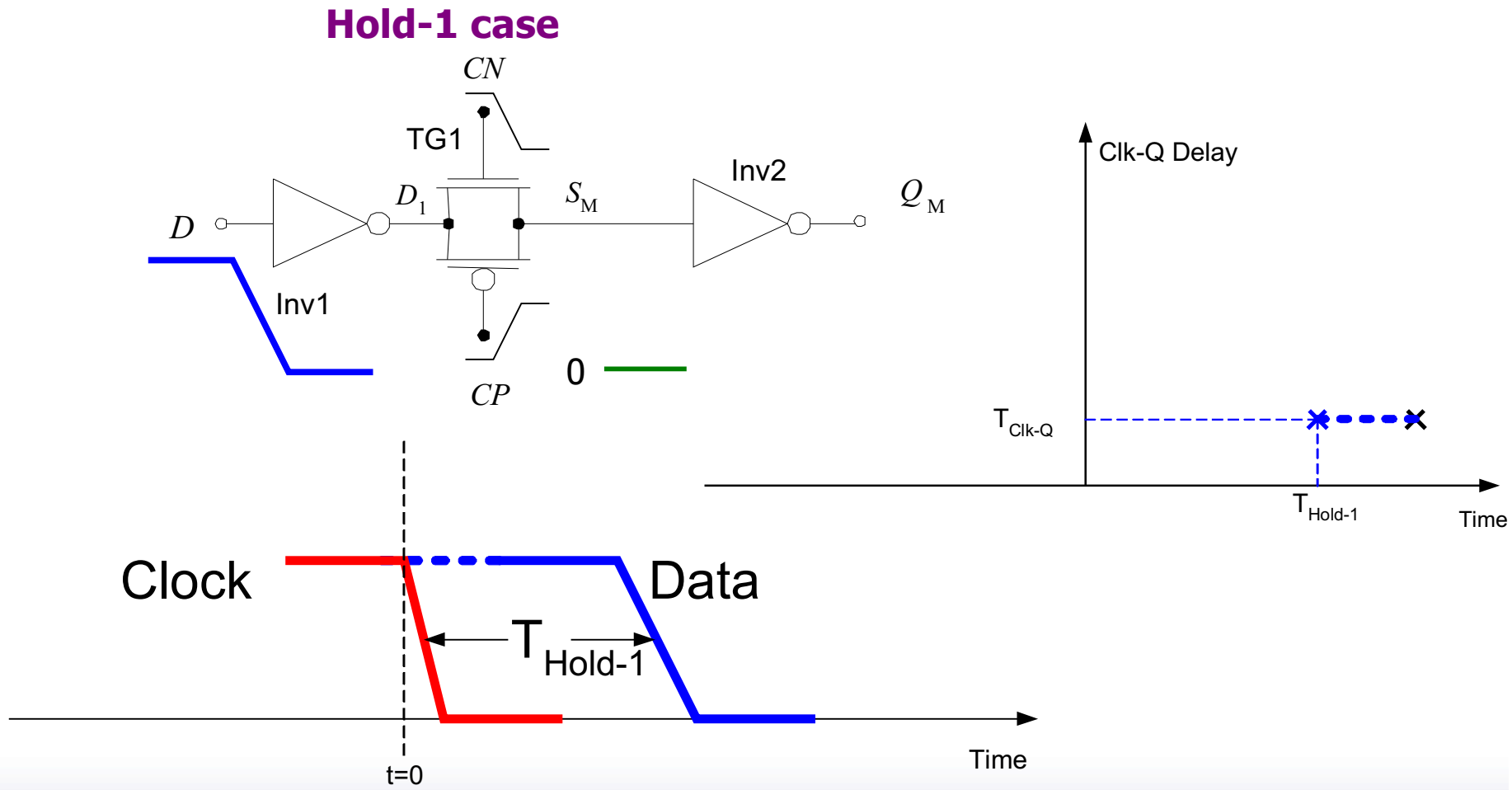
Circuit before clock arrival (Setup-1 case)



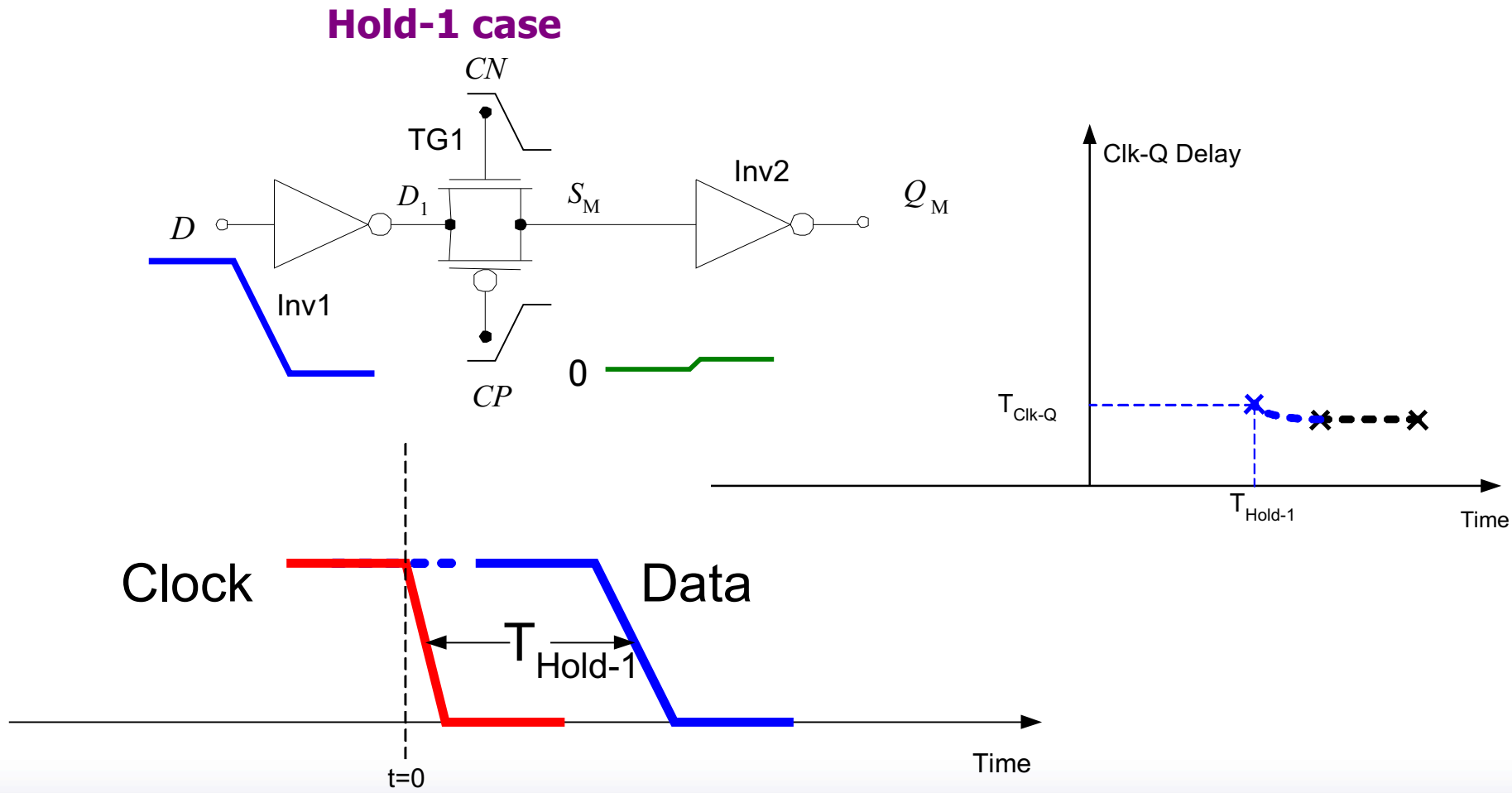
Setup/Hold Time Illustrations



Setup/Hold Time Illustrations



Setup/Hold Time Illustrations



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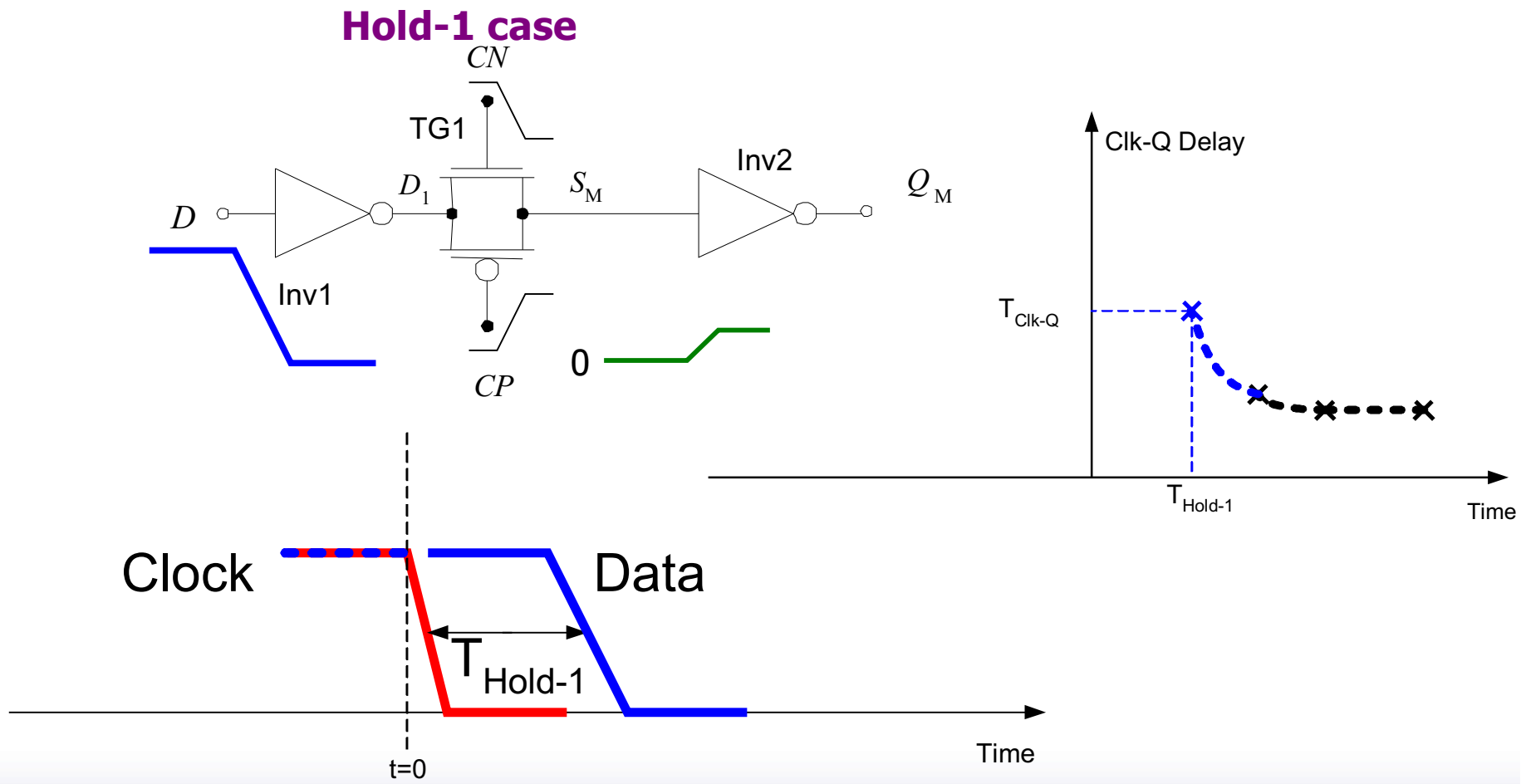
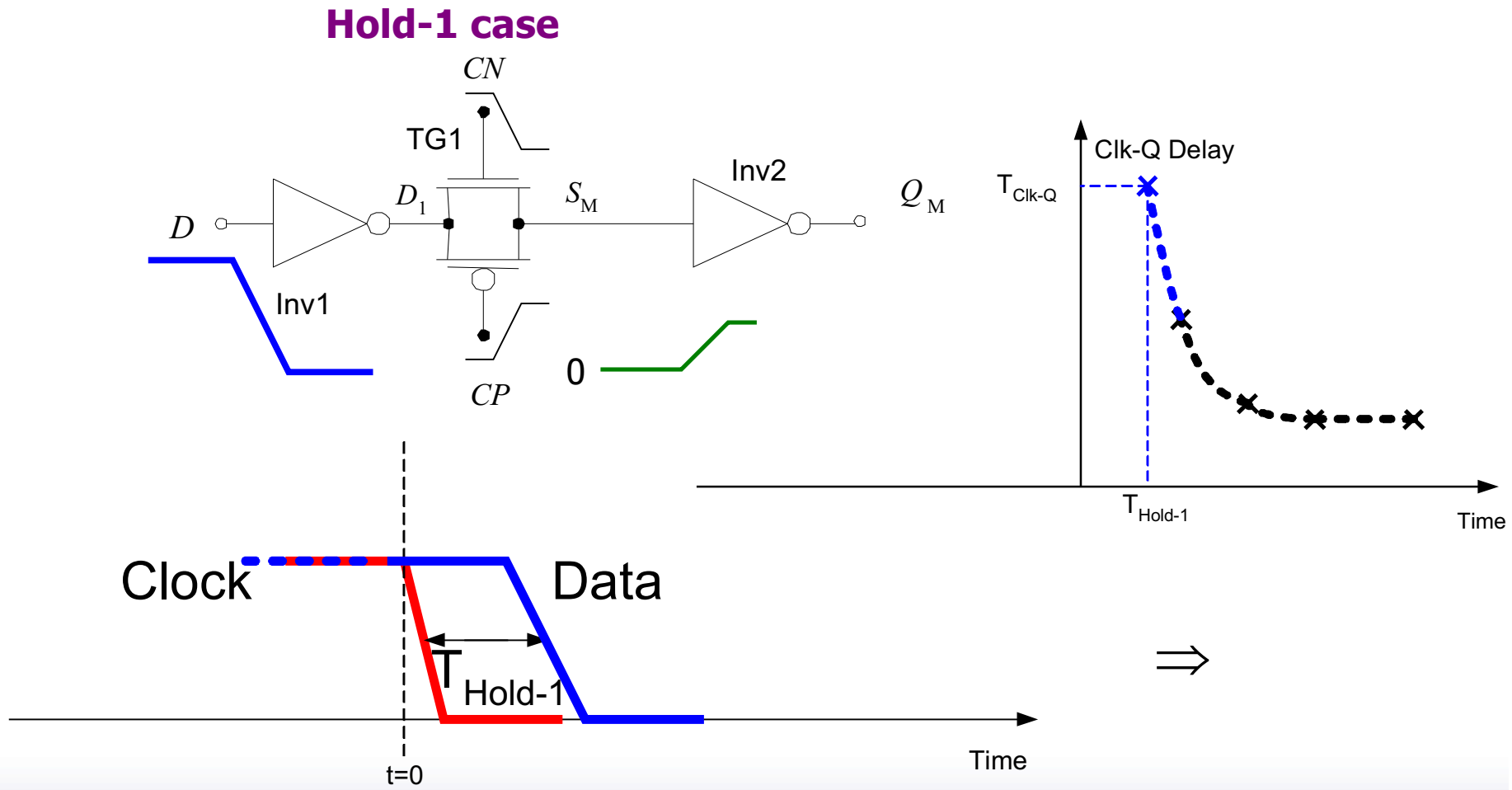
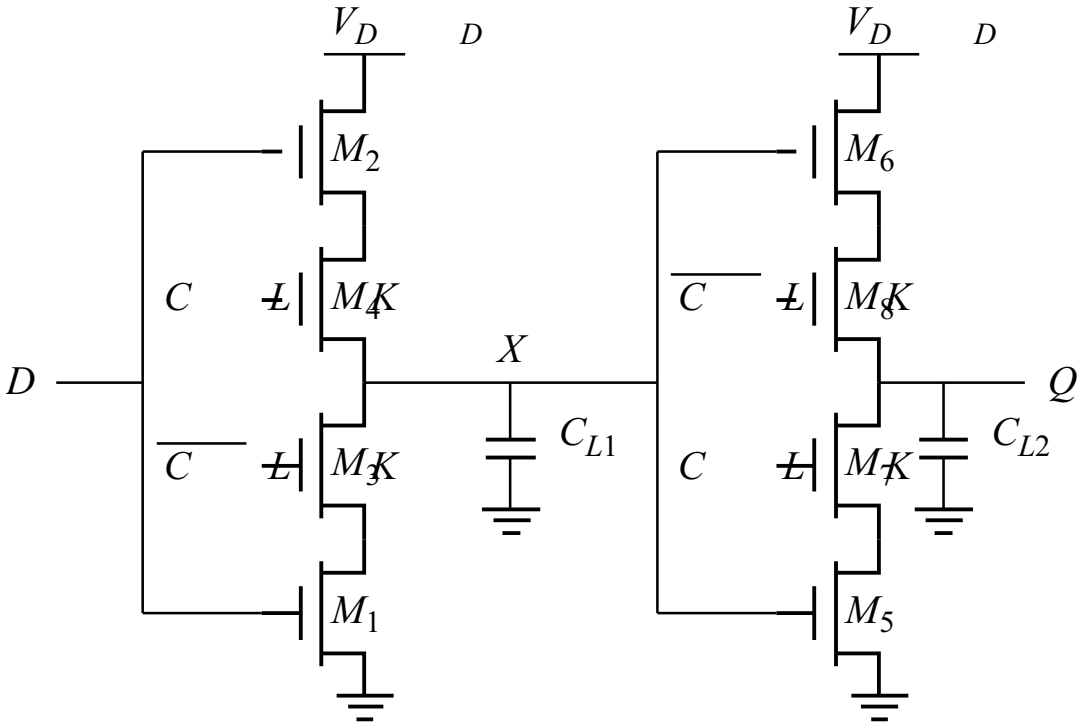


Setup/Hold Time Illustrations

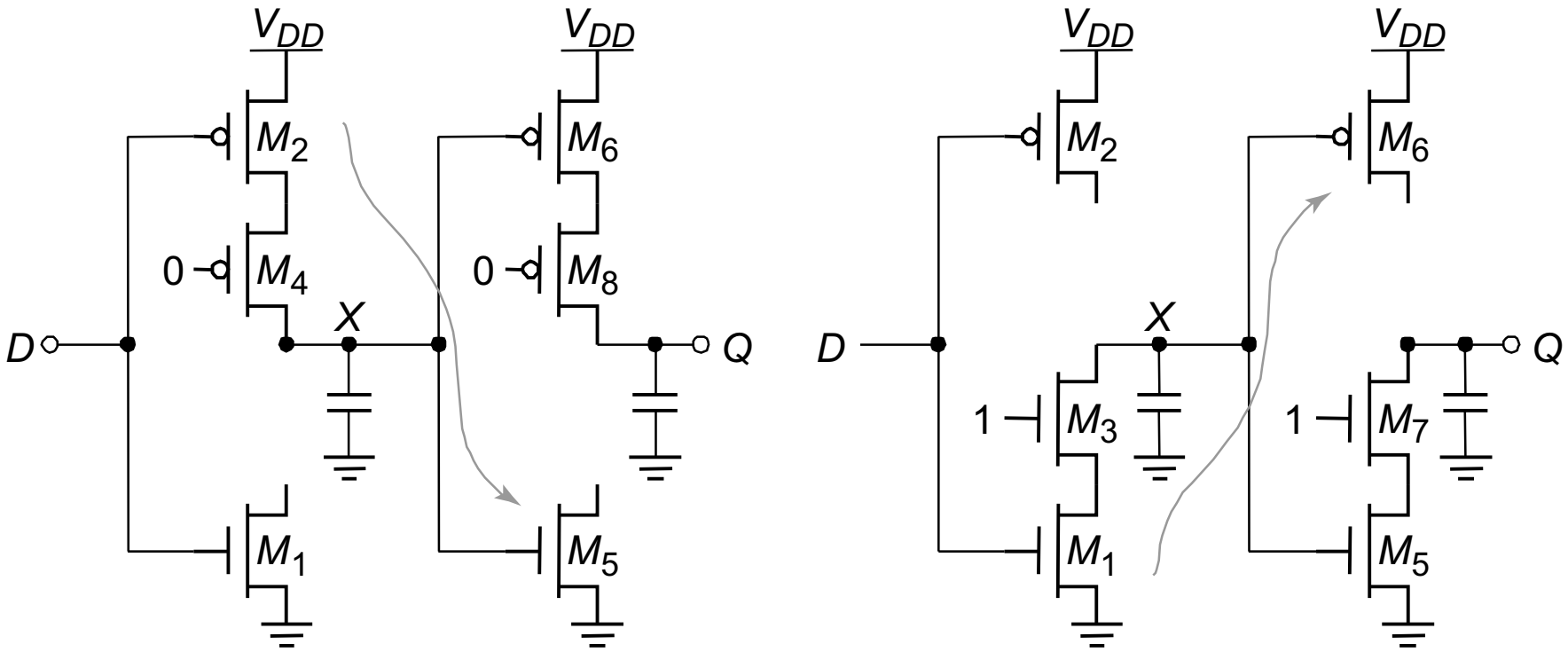


Other Latches/Registers: C²MOS



"Keepers" can be added to make circuit pseudo-static

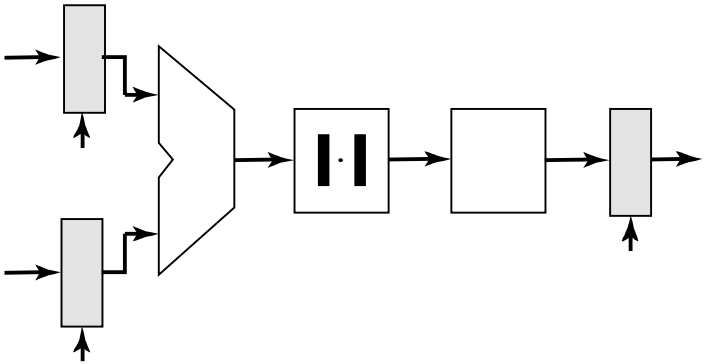
Insensitive to Clock-Overlap



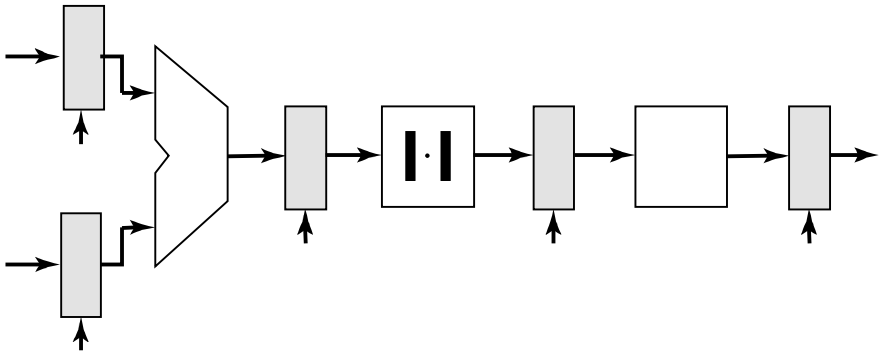
(a) (0-0) overlap

(b) (1-1) overlap

Pipelining



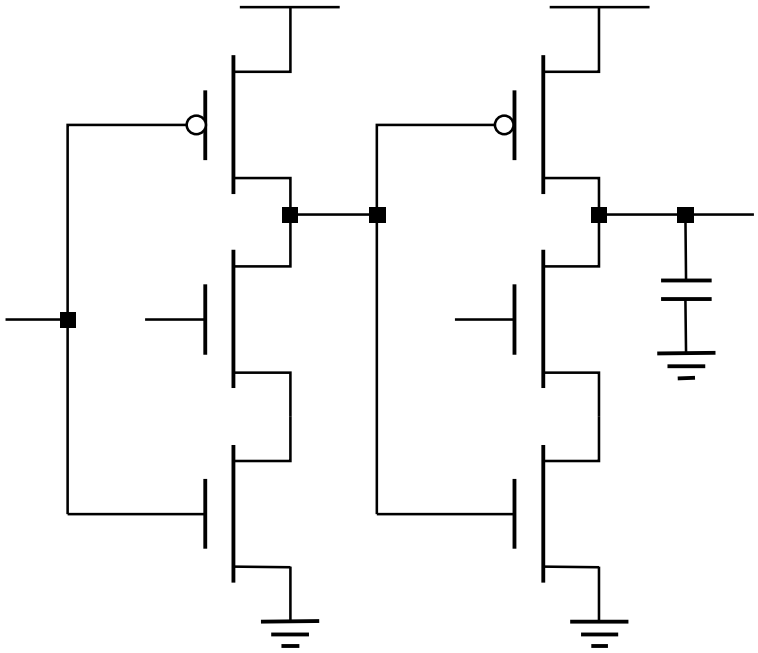
Reference



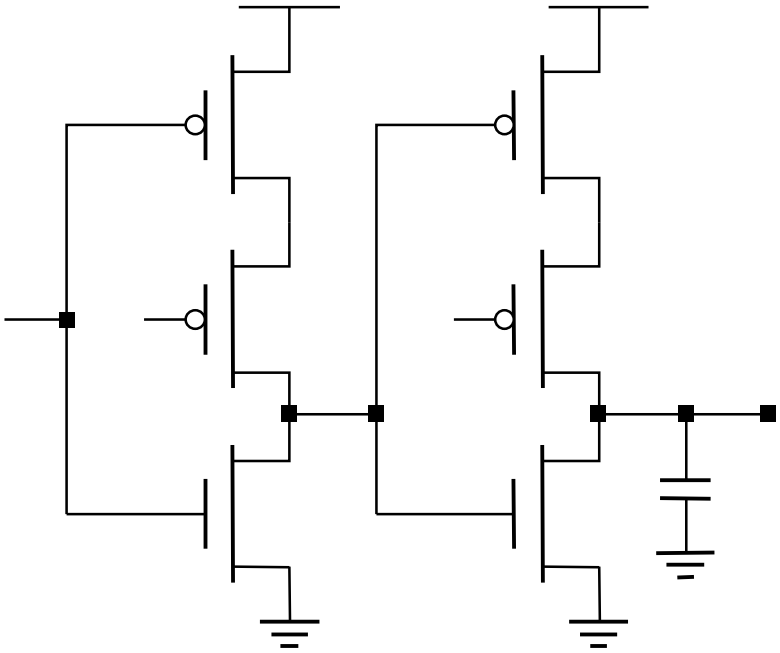
Pipelined

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\|a_1 + b_1\|$	
3	$a_3 + b_3$	$\|a_2 + b_2\|$	$\log(\|a_1 + b_1\|)$
4	$a_4 + b_4$	$\|a_3 + b_3\|$	$\log(\|a_2 + b_2\|)$
5	$a_5 + b_5$	$\|a_4 + b_4\|$	$\log(\|a_3 + b_3\|)$

Other Latches/Registers: TSPC



Positive latch
(transparent when CLK= 1)

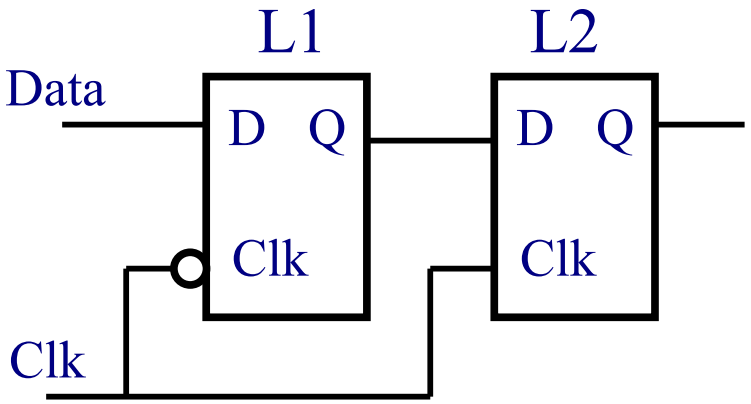


Negative latch
(transparent when CLK= 0)

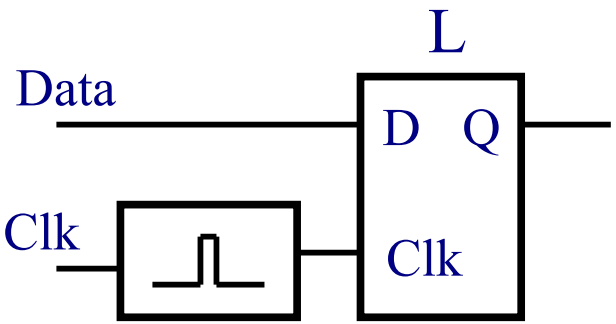
Pulse-Triggered Latches
An Alternative Approach

Ways to design an edge-triggered sequential cell:

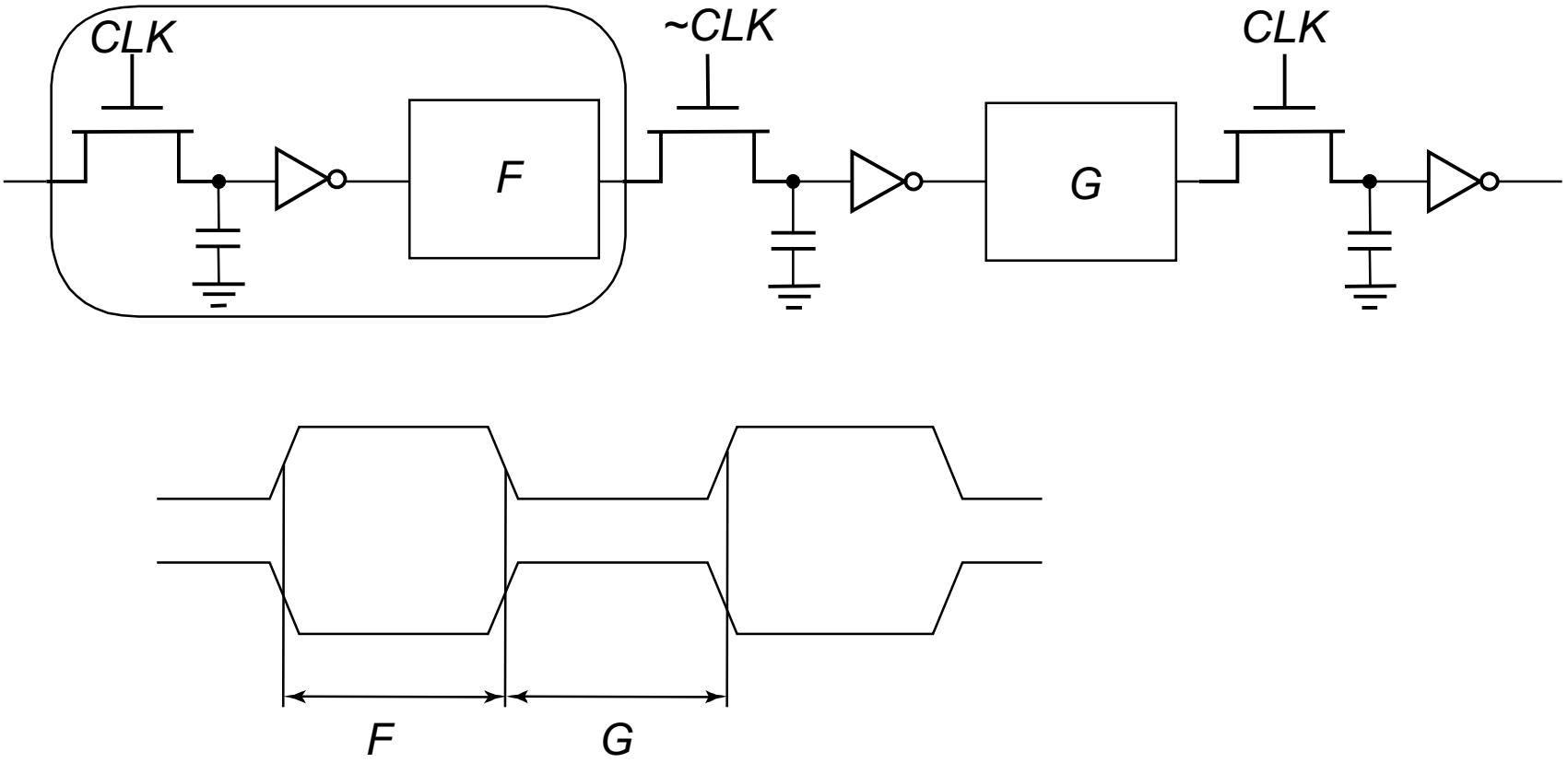
Master-Slave Latches



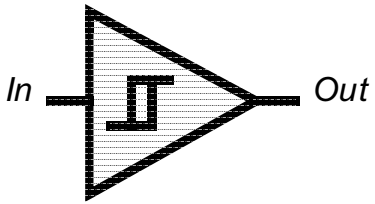
Pulse-Triggered Latch

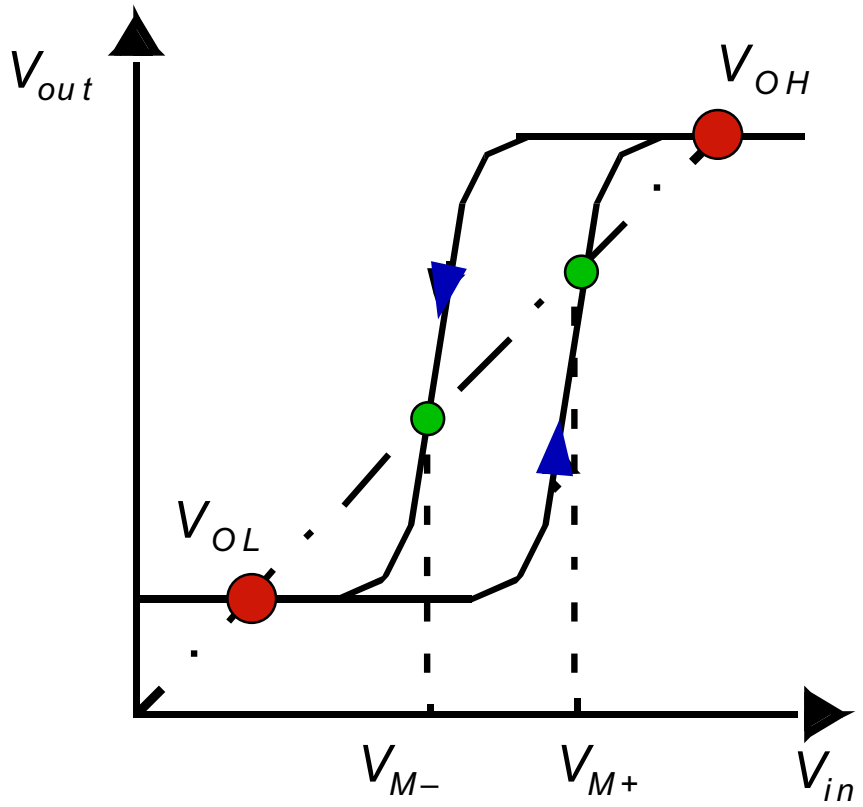


Latch-Based Pipeline



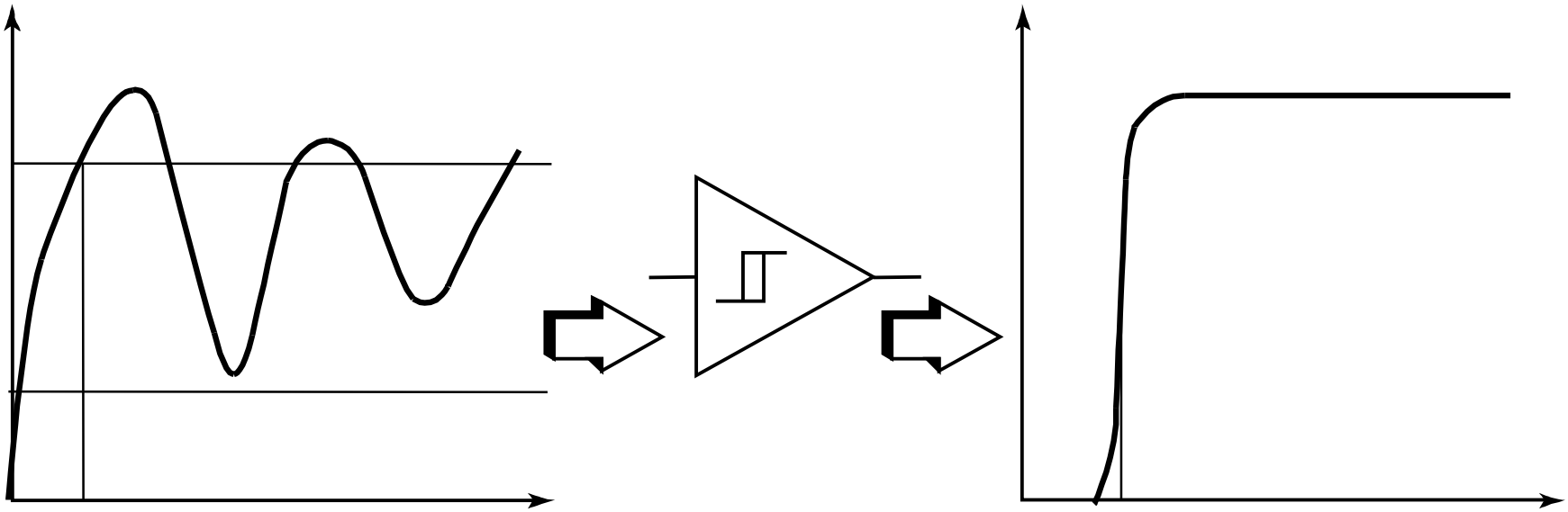
Non-Bistable Sequential Circuits—Schmitt Trigger



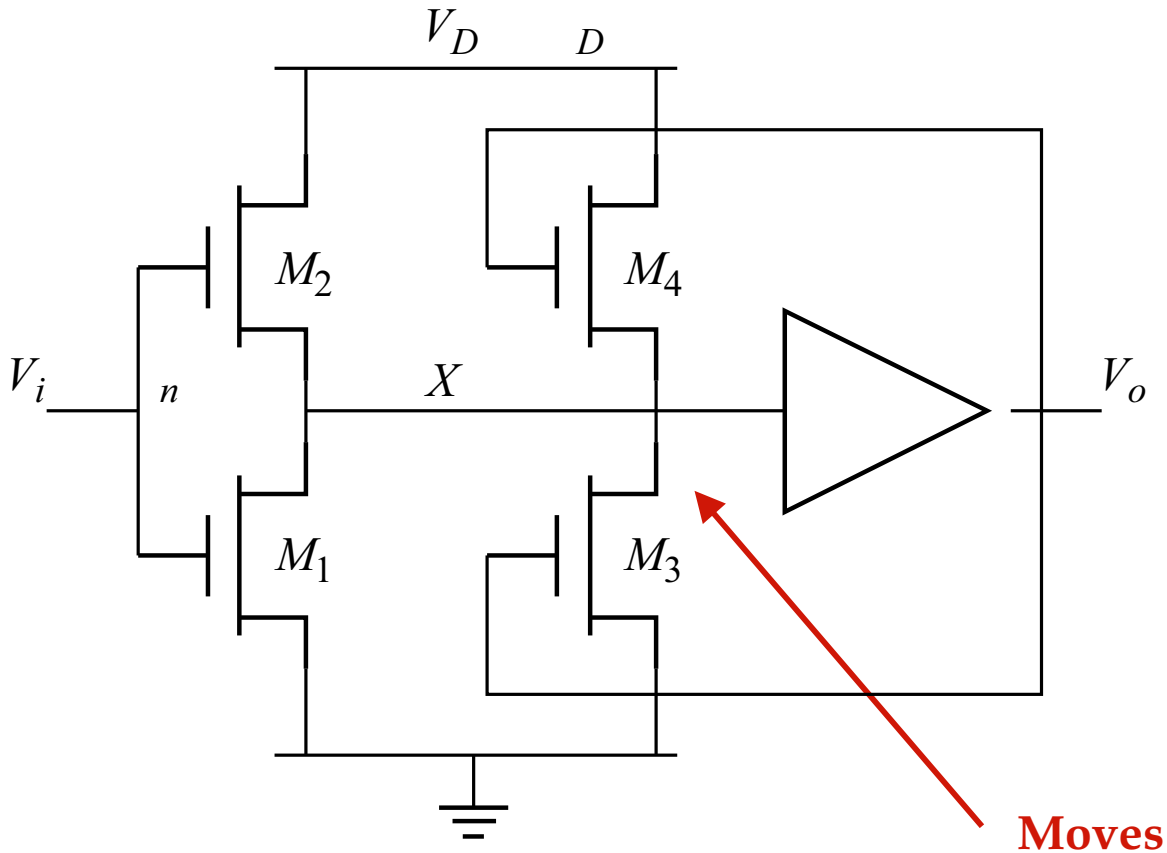


- VTC with hysteresis
- Restores signal slopes

Noise Suppression: Schmitt Trigger

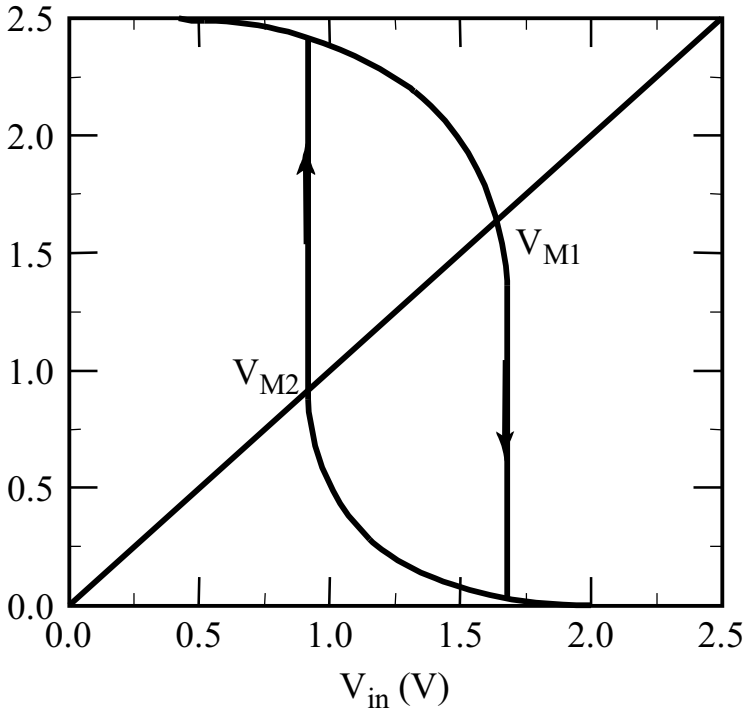


CMOS Schmitt Trigger

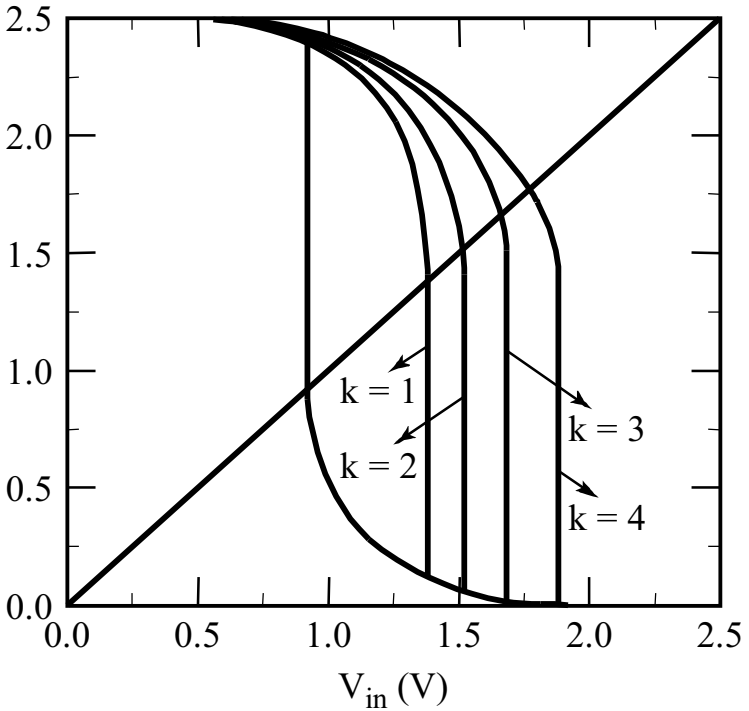


Moves switching threshold of the first inverter

Schmitt Trigger Simulated VTC

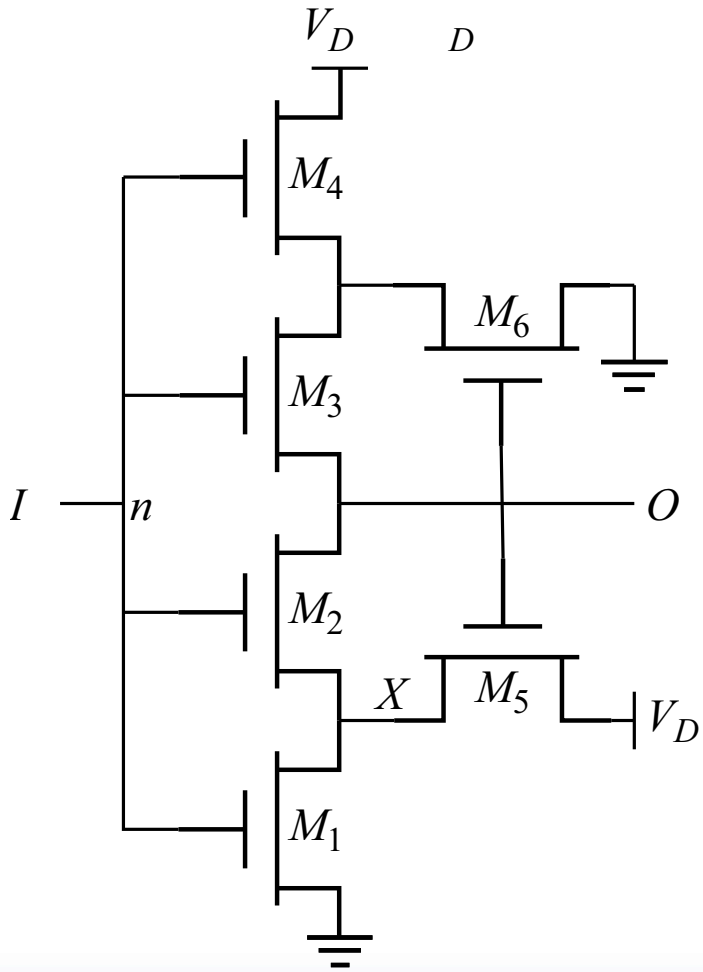


Voltage-transfer characteristics with hysteresis.

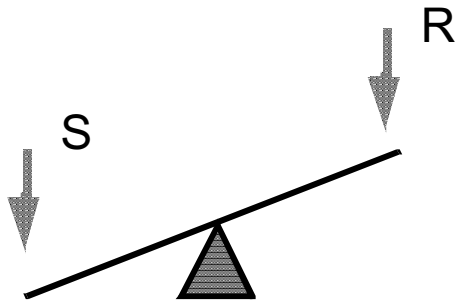


The effect of varying the ratio of the PMOS device M_4. The width is k* 0.5m m.

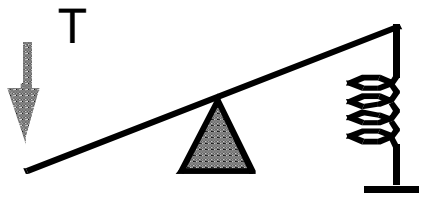
CMOS Schmitt Trigger (2)



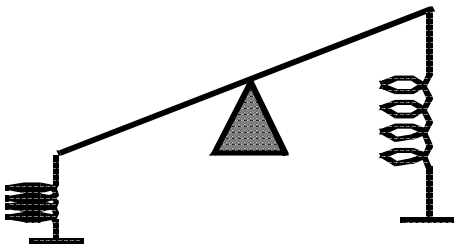
Multivibrator Circuits



Bistable Multivibrator
flip-flop, Schmitt Trigger

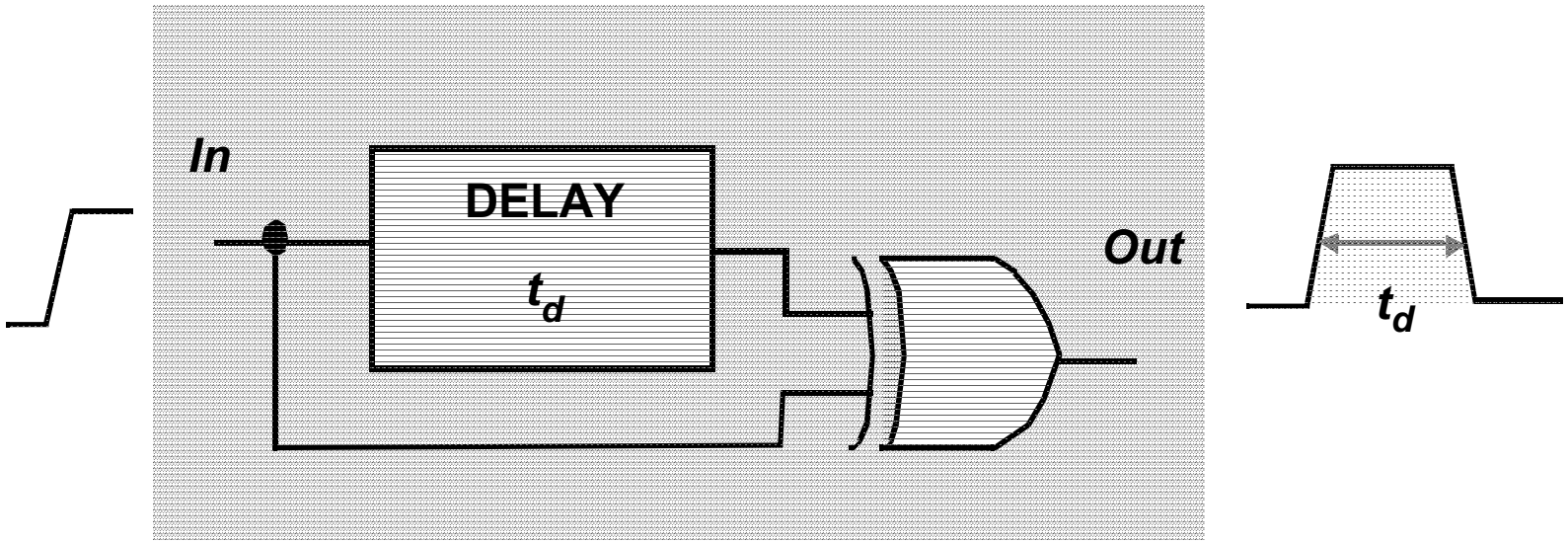


Monostable Multivibrator
one-shot

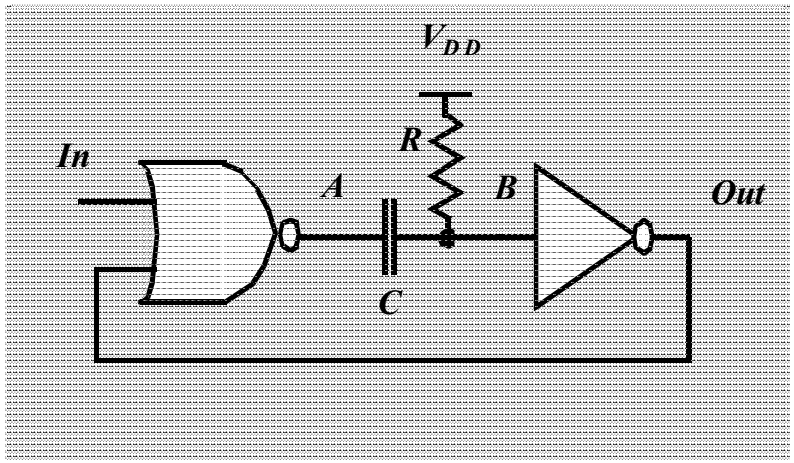


Astable Multivibrator
oscillator

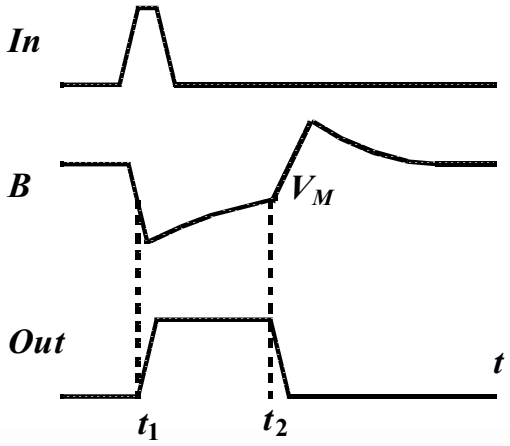
Transition-Triggered Monostable



Monostable Trigger (RC-based)

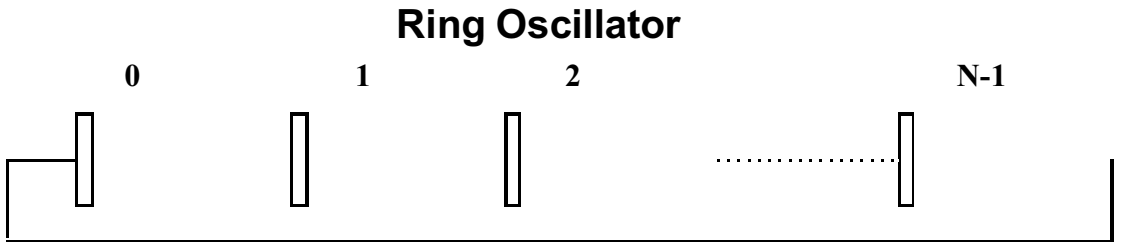


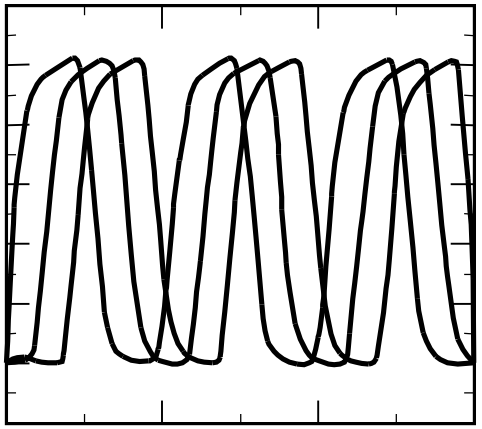
(a) Trigger circuit.



(b) Waveforms.

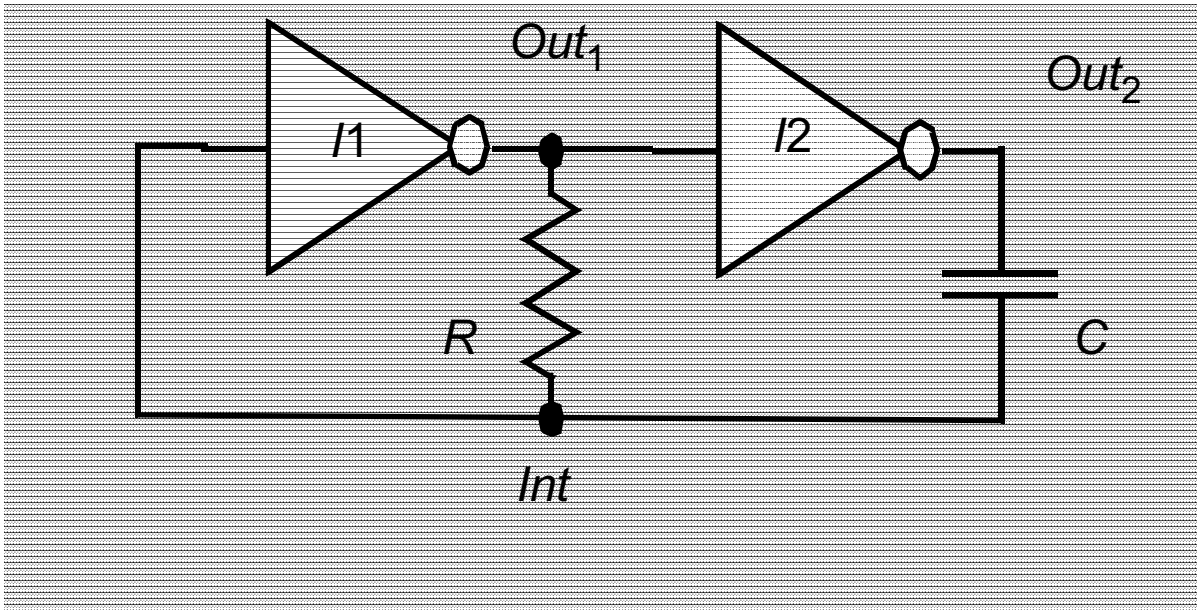
Astable Multivibrators (Oscillators)





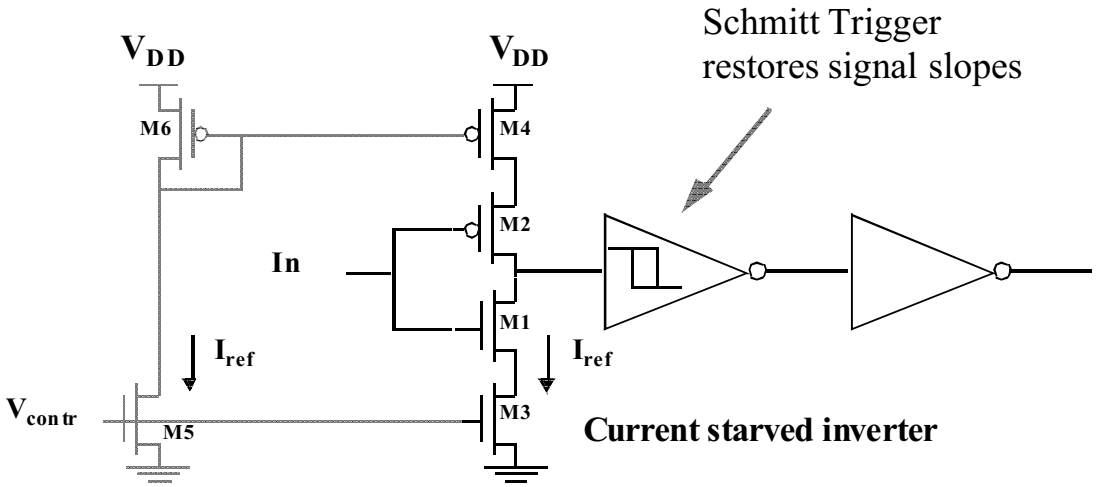
simulated response of 5-stage oscillator

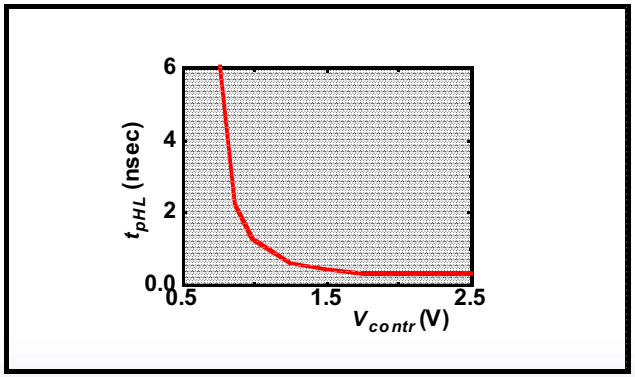
Relaxation Oscillator



$$T = 2\ (\log 3)\ RC$$

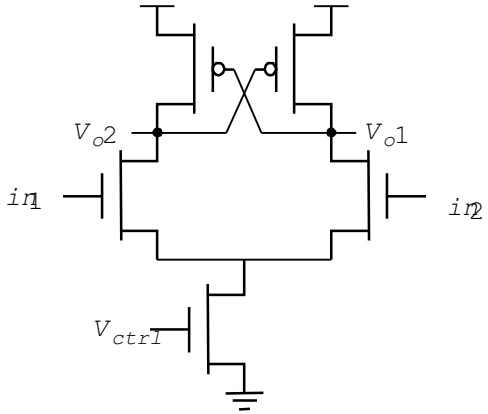
Voltage Controller Oscillator (VCO)



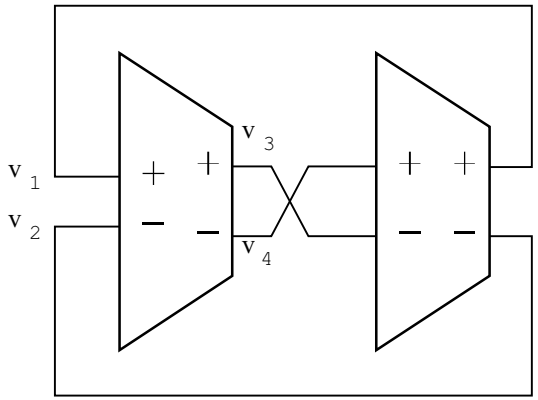


propagation delay as a function of control voltage

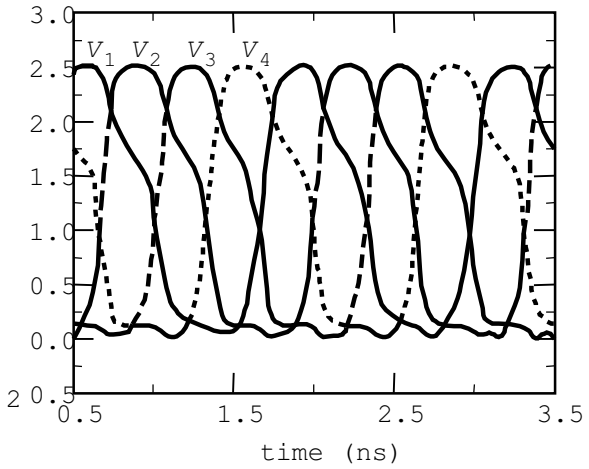
Differential Delay Element and VCO



delay cell



two stage VCO



simulated waveforms of 2-stage VCO

Homework 4

1. A common way to characterize registers is to measure the timing aperture which is the total window in which transitions on data are not correctly output. This is done by making two clocks which are close, but not the same so that the relative phase drifts slowley with each cycle. Construct a pseudo-static register, a C2MOS register, and a TSPC register in SUE with the assumption that the input is driven by a unit inverter (2/1, min width nmos), the clock is driven by a 2x inverter. Optimize your designs to minimize the timing aperture (setup+hold) and clock to Q assuming the output load is 2 inverters. Simulate your designs in SPICE and turn in both the designs (annotated schematics and spice results – plz. don't waste paper!)