Designing Combinational Logic Circuits: Part 2
Alternative Logic Forms:
Ratio Logic
Pass-Transistor
Dynamic Logic
Ratio Logic

(a) resistive load
(b) depletion load NMOS
(c) pseudo-NMOS

Goal: to reduce the number of devices over complementary CMOS
Ratio Logic

- N transistors + Load
- \( V_{OH} = V_{DD} \)
- \( V_{OL} = \frac{R_{PN}}{R_{PN} + R_L} \)
- Assymetrical response
- Static power consumption
- \( t_{PL} = 0.69 \ R_L C_L \)
Active Loads

Depletion Load

\[ V_{DD} \]
\[ V_{T} < 0 \]
\[ V_{SS} \]

In1
In2
In3

depletion load NMOS

PMOS Load

\[ V_{DD} \]
\[ V_{SS} \]
\[ V_{SS} \]

In1
In2
In3

pseudo-NMOS
**Pseudo-NMOS**

\[ V_{OH} = V_{DD} \text{ (similar to complementary CMOS)} \]

\[ k_n \left((V_{DD} - V_{Tn})V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{k_p}{2}(V_{DD} - |V_{Tp}|)^2 \]

\[ V_{OL} = (V_{DD} - V_T) \left[ 1 - \sqrt{1 - \frac{k_p}{k_n}} \right] \text{ (assuming that } V_T = V_{Tn} = |V_{Tp}| \)

**SMALLER AREA & LOAD BUT STATIC POWER DISSIPATION!!**

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Pseudo-NMOS VTC

![Graph showing VTC characteristics for different W/L ratios.](image)
Improved Loads

Adaptive Load
Even Better Noise Immunity

Differential Cascode Voltage Switch Logic (DCVSL)
DCVSL Example

XOR-NXOR gate
DCVSL Transient Response
Pass-Transistor Logic

- N transistors
- No static consumption
Example: AND Gate

\[ f = AB \]
NMOS-Only Logic

![Diagram of NMOS-Only Logic]

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NMOS-only Switch

$V_B$ does not pull up to 2.5V, but 2.5V -$V_{TN}$

Threshold voltage loss causes static power consumption

NMOS has higher threshold than PMOS (body effect)
**NMOS Only Logic:**
**Level Restoring Transistor**

- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem
Restorer Sizing

- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack
Solution 2: Single Transistor Pass Gate with $V_T=0$

WATCH OUT FOR LEAKAGE CURRENTS
Complementary Pass Transistor Logic

**Diagram (a):**
- **Pass-Transistor Network**
- **Inverse Pass-Transistor Network**
- Output expressions: $F = AB$, $F = A + B$, $F = A \oplus B$ (for AND/NAND, OR/NOR, EXOR/NEXOR)

**Diagram (b):**
- **Logic Gates**
- **Symbols**
- **Expressions**

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Solution 3: Transmission Gate

![Transmission Gate Diagram](image)
Resistance of Transmission Gate

![Graph showing the resistance of transmission gate](image)

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Pass-Transistor Based Multiplexer
Transmission Gate XOR

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Delay in Transmission Gate Networks

(a)

(b)

(c)
Delay Optimization

- Delay of RC chain

\[ t_p = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2} \]

- Delay of Buffered Chain

\[ t_p = 0.69 \left[ \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ = 0.69 \left[ CR_{eq} \frac{n(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ m_{opt} = 1.7 \sqrt{\frac{t_{pbu}}{CR_{eq}}} \]
Transmission Gate Full Adder

Setup

Sum Generation

Carry Generation

Similar delays for sum and carry
Dynamic Logic
Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or $V_{DD}$ via a low resistance path.
  - fan-in of $n$ requires $2n$ ($n$ N-type + $n$ P-type) devices

- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on $n + 2$ ($n+1$ N-type + 1 P-type) transistors
Dynamic Gate

Two phase operation
- Precharge (CLK = 0)
- Evaluate (CLK = 1)

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Dynamic Gate

Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)
Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on $C_L$.
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is $N + 2$ (versus $2N$ for static complementary CMOS)

- Full swing outputs ($V_{OL} = GND$ and $V_{OH} = V_{DD}$)

- Non-ratioed - sizing of the devices does not affect the logic levels

- Faster switching speeds
  - reduced load capacitance due to lower input capacitance ($C_{in}$)
  - reduced load capacitance due to smaller output loading ($C_{out}$)
  - no $I_{sc}$, so all the current provided by PDN goes into discharging $C_L$
Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between $V_{DD}$ and GND (including $P_{sc}$)
  - no glitching
  - higher transition probabilities
  - extra load on Clk

- PDN starts to work as soon as the input signals exceed $V_{Tn}$, so $V_M$, $V_{IH}$ and $V_{IL}$ equal to $V_{Tn}$
  - low noise margin ($NM_L$)

- Needs a precharge/evaluate clock
Issues in Dynamic Design 1: Charge Leakage

Leakage sources

Dominant component is subthreshold current
Solution to Charge Leakage

Same approach as level restorer for pass-transistor logic
Issues in Dynamic Design 2: Charge Sharing

Charge stored originally on $C_L$ is redistributed (shared) over $C_L$ and $C_A$ leading to reduced robustness
Charge Sharing Example

\[ C_a = 15\text{fF} \]
\[ C_c = 15\text{fF} \]
\[ C_b = 15\text{fF} \]
\[ C_d = 10\text{fF} \]

Out \( C_L = 50\text{fF} \)
Charge Sharing

**Case 1** if $\Delta V_{out} < V_{Tn}$

\[ C_L V_{DD} = C_L V_{out}(t) + C_a (V_{DD} - V_{Tn}(V_X)) \]

or

\[ \Delta V_{out} = V_{out}(t) - V_{DD} = \frac{C_a}{C_L} (V_{DD} - V_{Tn}(V_X)) \]

**Case 2** if $\Delta V_{out} > V_{Tn}$

\[ \Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right) \]
Solution to Charge Redistribution

Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)
Issues in Dynamic Design 3: Backgate Coupling

Dynamic NAND

Static NAND

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Issues in Dynamic Design 4: Clock Feedthrough

Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above $V_{DD}$. The fast rising (and falling edges) of the clock couple to Out.
Clock Feedthrough

![Diagram showing clock feedthrough](image)

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Other Effects

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)
Cascading Dynamic Gates

Only 0 → 1 transitions allowed at inputs!
Domino Logic

```
Clk  M_p  1 → 1
     1 → 0

In_1
In_2
In_3

PDN

Clk  M_e

Out1

```

```
Clk  M_p  Mkp

In_4
In_5

PDN

Clk  M_e

Out2
```
Why Domino?

Like falling dominos!
Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition
  - Input capacitance reduced – smaller logical effort
Designing with Domino Logic

Can be eliminated!

Inputs = 0 during precharge
Footless Domino

The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current
A solution is to delay the clock for each stage
Differential (Dual Rail) Domino

Out = \overline{AB}

Solves the problem of non-inverting logic
np-CMOS

Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN
NORA Logic

WARNING: Very sensitive to noise!

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Homework 6

1. Design (in Sue) a CPL version of the 16-bit ripple adder using transistors from the AMI 0.6 process. Simulate in Hspice and measure the worst case delay and average power/MHz.

2. Design (in Sue and simulate) a Domino version of the same ripple adder – measure the w.c. delay and average power/MHz.

(How do these designs compare to Static CMOS?)