CMOS Inverter: Digital Workhorse

- Best Figures of Merit in CMOS Family
  - Noise Immunity
  - Performance
  - Power/Buffer Ability
  - Utilization of Design Scale

- Maxim
  - When in doubt – add an inverter!
CMOS Inverter

\[ V_{DD} \]

\[ \text{PMOS} \]

\[ \text{NMOS} \]

\[ \text{In} \]

\[ \text{Out} \]

N Well

PMOS

Contacts

Polysilicon

NMOS

GND

\[ V_{DD} \]

\[ \text{In} \]

\[ \text{Out} \]

Metal 1

\[ 2\lambda \]

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Inverter
CMOS Inverter Load Characteristics

$I_{D_{n}}$  $V_{in} = 0$  $V_{in} = 2.5$

PMOS

$V_{in} = 0.5$  $V_{in} = 2$

$V_{in} = 1.5$  $V_{in} = 1.5$

$V_{in} = 2$  $V_{in} = 1$

$V_{in} = 2.5$  $V_{in} = 0.5$

$V_{out}$

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CMOS Inverter VTC
Low Frequency Switching Threshold vs. Transistor Ratio

\[ k_n V_{DSATn} \left( V_M - V_{Th} - \frac{V_{DSATn}}{2} \right) + k_p V_{DSATp} \left( V_M - V_{DD} - V_{Th} - \frac{V_{DSATp}}{2} \right) = 0 \]

Solving for \( V_M \) yields

\[ V_M = \frac{\left( V_{Th} + \frac{V_{DSATn}}{2} \right) + r \left( V_{DD} + V_{Th} + \frac{V_{DSATp}}{2} \right)} {1 + r} \]

with

\[ r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{satin} W_n} \]

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\[ V_M (V) \]

\[ W_p / W_n \]
Inverter Gain

\[ g = \frac{1}{I_D(V_M)} \left( \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \right) \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)} \]
Gain as a function of VDD

Gain=-1
Simulated VTC

![Graph showing simulated VTC for an inverter circuit.](image)
Impact of Process Variations I

![Graph showing impact of process variations on an inverter circuit.](image-url)

- Fast PMOS
- Slow NMOS
- Typical
- Fast NMOS
- Slow PMOS

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Inverter
Impact of Process Variations II

- Inverter Noise Margin
  - Directly limited by Process Variations
  - Also Function of Gain, Power Rail Noise, Temp
Propagation Delay
CMOS Inverter: RC Transient Response Model

- Assume Next Gate Switches at 50% swing
- Total Delay from sum of sequential gate delays

$t_{pHL} = f(R_{on} \cdot C_L) = 0.69 R_{on} C_L$
CMOS Inverter Propagation Delay
RC Approximation

\[ t_{pHL} = f(R_{on} \cdot C_L) \]
\[ = 0.69 \, R_{on} C_L \]
Transitent Response (Equivalent $R$)

\[ R_{eq} = \frac{1}{V_{DD}/2} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)} dV \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9} \lambda V_{DD}\right) \]

with \[ I_{DSAT} = \frac{W}{L} \left((V_{DD} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2}\right) \]
CMOS Inverter Propagation Delay
Hodges Approximation

\[
t_{\text{pHL}} = \frac{C_L}{I_{\text{av}}} \left( \frac{V_{\text{swing}}}{2} \right)
\]

\[
\sim \frac{C_L}{k_n V_{\text{DD}}}
\]

\[V_{\text{in}} = V_{\text{DD}}\]
Transient Model (Equivalent I)

- Hodges Perscription for $I_{avg}$:
  - Average of Initial and Final Currents over swing of interest
  - Easy since you know the voltages in CMOS: Init=0 or Vdd; Final= Vdd/2
  - Easy to add effects of other devices, capacitances and styles since current model
Device Sizing

For fixed load: Intrinsic capacitances dominate.

Self-loading effect: Intrinsically dominant.
Issues in Propagation Estimation

- Critical Path??
  - Transitions are critical
  - Asymmetric transistor sizing may be good!
  - Dial in Noise/Level Shift/Favored Transition

- Load
  - Interconnect
  - Terminal
  - Self-loading (non-linear)

- Output Swing
  - Usually Vdd->Vdd/2 or GND->Vdd/2
NMOS/PMOS ratio

\[ \beta = \frac{W_p}{W_n} \]
Propagation Details

- Most of Load is simple, but:
  - Non-linear Self Capacitance
    - Drain Junction and Sidewalls
  - Ratio Logic
    - Other current sources/sinks

- Beware Body Effect
  - Source at different potential from back
Impact of Rise Time on Delay

\[ t_{pHL} = \sqrt{t_{pHL\text{ (step)}} + (t_r/2)^2} \]
Inverter Sizing
Inverter Chain

If $C_L$ is given:
- How many stages are needed to minimize the delay?
- How to size the inverters?

May need some additional constraints.
**Inverter Delay**

- Minimum length devices, L=0.5μm
- Assume that for $W_P = 2.5W_N = 2.5W$
  - same pull-up and pull-down currents
  - approx. equal resistances $R_N = R_P$
  - approx. equal rise $t_{pLH}$ and fall $t_{pHL}$ delays
- Analyze as an RC network

\[
R_P = R_{unit} \left( \frac{W_P}{W_{unit}} \right)^{-1} \approx R_{unit} \left( \frac{W_N}{W_{unit}} \right)^{-1} = R_N = R_W
\]

Delay ($D$): $t_{pHL} = (\ln 2) R_N C_L$  
$t_{pLH} = (\ln 2) R_P C_L$

Load for the next stage:  
\[
C_{gin} = 3 \frac{W}{W_{unit}} C_{unit}
\]
**Inverter with Load**

\[ t_p = k R_W C_L \]

- \( k \) is a constant, equal to 0.69
- Assumptions: no load -> zero delay
  \[ W_{\text{unit}} = 1 \]
Inverter with Load

\[ C_P = 2.5C_{\text{unit}} \]

\[ C_N = C_{\text{unit}} \]

\[ W \]

\[ C_{\text{int}} \]

\[ C_L \]

Delay = \[ kR_W(C_{\text{int}} + C_L) = kR_W C_{\text{int}} + kR_W C_L = kR_W C_{\text{int}}(1 + \frac{C_L}{C_{\text{int}}}) \]

= Delay (Internal) + Delay (Load)
Delay Formula

\[ \text{Delay} \sim R_W \left| C_{\text{int}} + C_L \right| \]

\[ t_p = kR_W C_{\text{int}} \left| 1 + \frac{C_L}{C_{\text{int}}} \right| = t_{p0} \left| 1 + \frac{f}{\gamma} \right| \]

\[ C_{\text{int}} = \gamma C_{\text{gin}} \text{ with } \gamma \approx 1 \]
\[ f = \frac{C_L}{C_{\text{gin}}} - \text{effective fanout} \]
\[ R = \frac{R_{\text{unit}}}{W} ; C_{\text{int}} = WC_{\text{unit}} \]
\[ t_{p0} = 0.69R_{\text{unit}} C_{\text{unit}} \]
Apply to Inverter Chain

\[ t_p = t_{p1} + t_{p2} + \ldots + t_{pN} \]

\[ t_{pj} \sim R_{\text{unit}} C_{\text{unit}} \left( 1 + \frac{C_{\text{gin},j+1}}{\gamma C_{\text{gin},j}} \right) \]

\[ t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{i=1}^{N} \left( 1 + \frac{C_{\text{gin},j+1}}{\gamma C_{\text{gin},j}} \right), \quad C_{\text{gin},N+1} = C_L \]
Optimal Sizing for Given N

Delay equation has \( N - 1 \) unknowns, \( C_{\text{gin},2} - C_{\text{gin},N} \)

Minimize the delay, find \( N - 1 \) partial derivatives

Result: \( C_{\text{gin},j+1}/C_{\text{gin},j} = C_{\text{gin},j}/C_{\text{gin},j-1} \)

Size of each stage is the geometric mean of two neighbors

\[
C_{\text{gin},j} = \sqrt{C_{\text{gin},j-1}C_{\text{gin},j+1}}
\]

- each stage has the same effective fanout \( (C_{\text{out}}/C_{\text{in}}) \)
- each stage has the same delay
Optimum Delay and Number of Stages

When each stage is sized by $f$ and has same fanout $f$:

$$f^N = F = \frac{C_L}{C_{gin,1}}$$

Effective fanout of each stage:

$$f = \sqrt[N]{F}$$

Minimum path delay

$$t_p = Nt_{p0} \left| 1 + \frac{N\sqrt{F}}{\gamma} \right|$$
Example

![Circuit Diagram]

\( C_L / C_1 \) has to be evenly distributed across \( N = 3 \) stages:

\[
f = \sqrt[3]{8} = 2
\]
Optimum Number of Stages

For a given load, $C_L$ and given input capacitance $C_{in}$
Find optimal sizing $f$

$$C_L = F \cdot C_{in} = f^N C_{in} \quad \text{with} \quad N = \frac{\ln F}{\ln f}$$

$$t_p = N t_{p0} \left| F^{1/N} / \gamma + 1 \right| = \frac{t_{p0} \ln F}{\gamma} \left( \frac{f}{\ln f} + \frac{\gamma}{\ln f} \right)$$

$$\frac{\partial t_p}{\partial f} = \frac{t_{p0} \ln F}{\gamma} \cdot \frac{\ln f - 1 - \gamma / f}{\ln^2 f} = 0$$

For $\gamma = 0$, $f = e$, $N = \ln F$

$$f = \exp \left| 1 + \gamma / f \right|$$
Optimum Effective Fanout $f$

Optimum $f$ for given process defined by $\gamma$

$$f = \exp\left(1 + \frac{\gamma}{f}\right)$$

$f_{opt} = 3.6$

for $\gamma = 1$
Impact of Self-Loading on $tp$

No Self-Loading, $\gamma=0$  

With Self-Loading $\gamma=1$
Buffer Design

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Power Dissipation
Where Does Power Go in CMOS?

- **Dynamic Power Consumption**
  Charging and Discharging Capacitors

- **Short Circuit Currents**
  Short Circuit Path between Supply Rails during Switching

- **Leakage**
  Leaking diodes and transistors
Dynamic Power Dissipation

\[
\text{Energy/transition} = C_L \times V_{dd}^2 \\
\text{Power} = \text{Energy/transition} \times f = C_L \times V_{dd}^2 \times f
\]

- Not a function of transistor sizes!
- Need to reduce $C_L$, $V_{dd}$, and $f$ to reduce power.
Transistor Sizing for Minimum Energy

- Goal: Minimize Energy of whole circuit
  - Design parameters: \( f \) and \( V_{DD} \)
  - \( tp \leq t_{pref} \) of circuit with \( f=1 \) and \( V_{DD} = V_{ref} \)

\[
t_p = t_{p0}\left(\frac{1 + \frac{f}{\gamma}}{1 + \frac{F}{f\gamma}}\right)
\]

\[
t_{p0} \propto \frac{V_{DD}}{V_{DD} - V_{TE}}
\]
Transistor Sizing (2)

- Performance Constraint ($\gamma=1$)

\[
\frac{t_p}{t_{p0}} = \frac{3 + F}{3 + F} \left(2 + f + \frac{F}{f}\right) = \frac{V_{DD}}{V_{ref}} \frac{V_{ref} - V_{TE}}{V_{DD} - V_{TE}} \left(2 + f + \frac{F}{f}\right) = 1
\]

- Energy for single Transition

\[
E = V_{DD}^2 C_{g1} \left|1 + \gamma \left|1 + f\right| + F\right|
\]

\[
\frac{E}{E_{ref}} = \left(\frac{V_{DD}}{V_{ref}}\right)^2 \left(\frac{2 + 2f + F}{4 + F}\right)
\]
Transistor Sizing (3)

\[ V_{DD} = f(f) \]

\[ E/E_{ref} = f(f) \]
Short Circuit Currents

Vin

\[ V_{dd} \]

\[ C_L \]

Vout

\[ V_{in} \ (V) \]

\[ I_{DC} \ (mA) \]
How to keep Short-Circuit Currents Low?

Short circuit current goes to zero if $t_{\text{fall}} \gg t_{\text{rise}}$, but can’t do this for cascade logic, so ...

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Inverter
Minimizing Short-Circuit Power

- Keep the input and output rise/fall times the same (< 10% of Total Consumption) from [Veendrick84]

(IEEE Journal of Solid-State Circuits, August 1984)

- If $V_{dd} < V_{tn} + |V_{tp}|$ then short-circuit power can be eliminated!
Sub-threshold current one of most compelling issues in low-energy circuit design!
Reverse-Biased Diconic Leakage

\[ I_{DL} = J_S \times A \]

\[ J_S = 10-100 \text{ pA/\(\mu\text{m}^2\)} \text{ at 25 deg C for 0.25\(\mu\text{m}\) CMOS} \]

\[ J_S \text{ doubles for every 9 deg C!} \]
Subthreshold Leakage Component

- Leakage control is critical for low-voltage operation
Principles for Power Reduction

- **Prime choice: Reduce voltage!**
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 ... 0.9 V by 2010!)

- **Reduce switching activity**

- **Reduce physical capacitance**
  - Device Sizing: for $F=20$
    - $f_{opt}$(energy) = 3.53, $f_{opt}$(performance) = 4.47