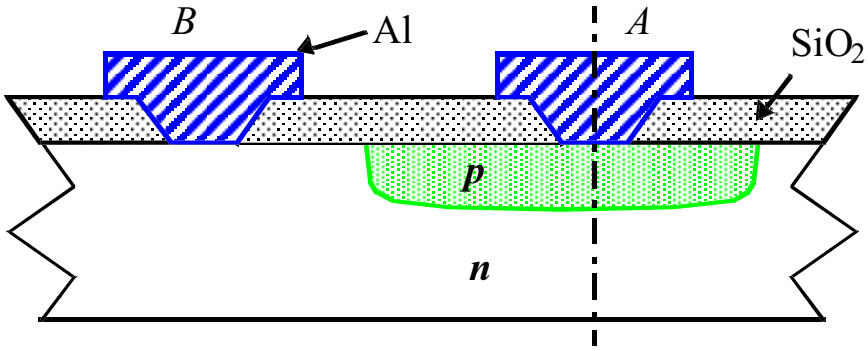
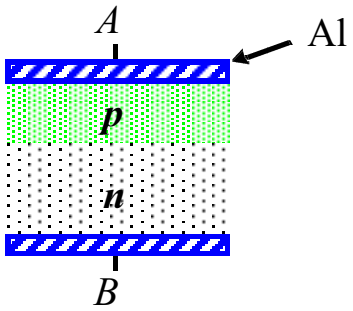
VLSI Devices

- Intuitive understanding of device operation
- Fundamental analytic models
  - Manual Models
  - Spice Models
- Secondary and deep-sub-micron effects
- Junction Diode and FET
- Resistor and Capacitor

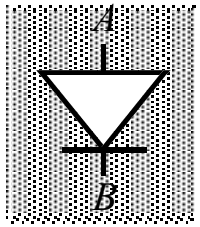
The Diode



Cross-section of *pn*-junction in an IC process



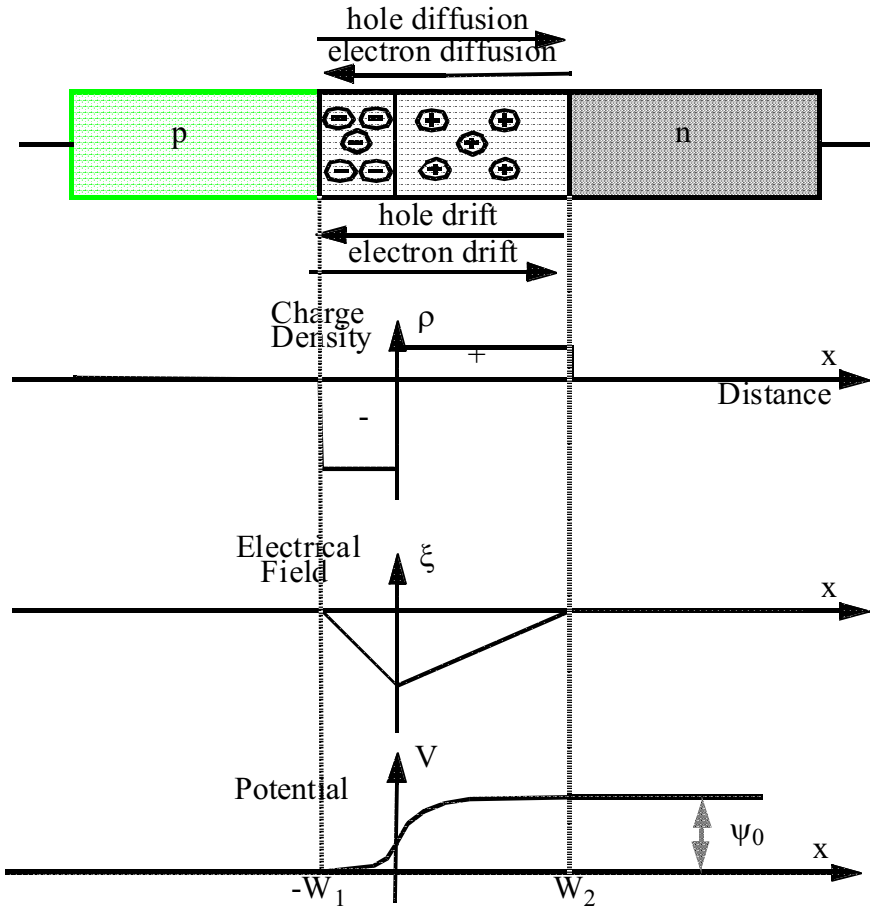
One-dimensional representation



diode symbol

Occurs as parasitic element in Digital ICs

Depletion Region



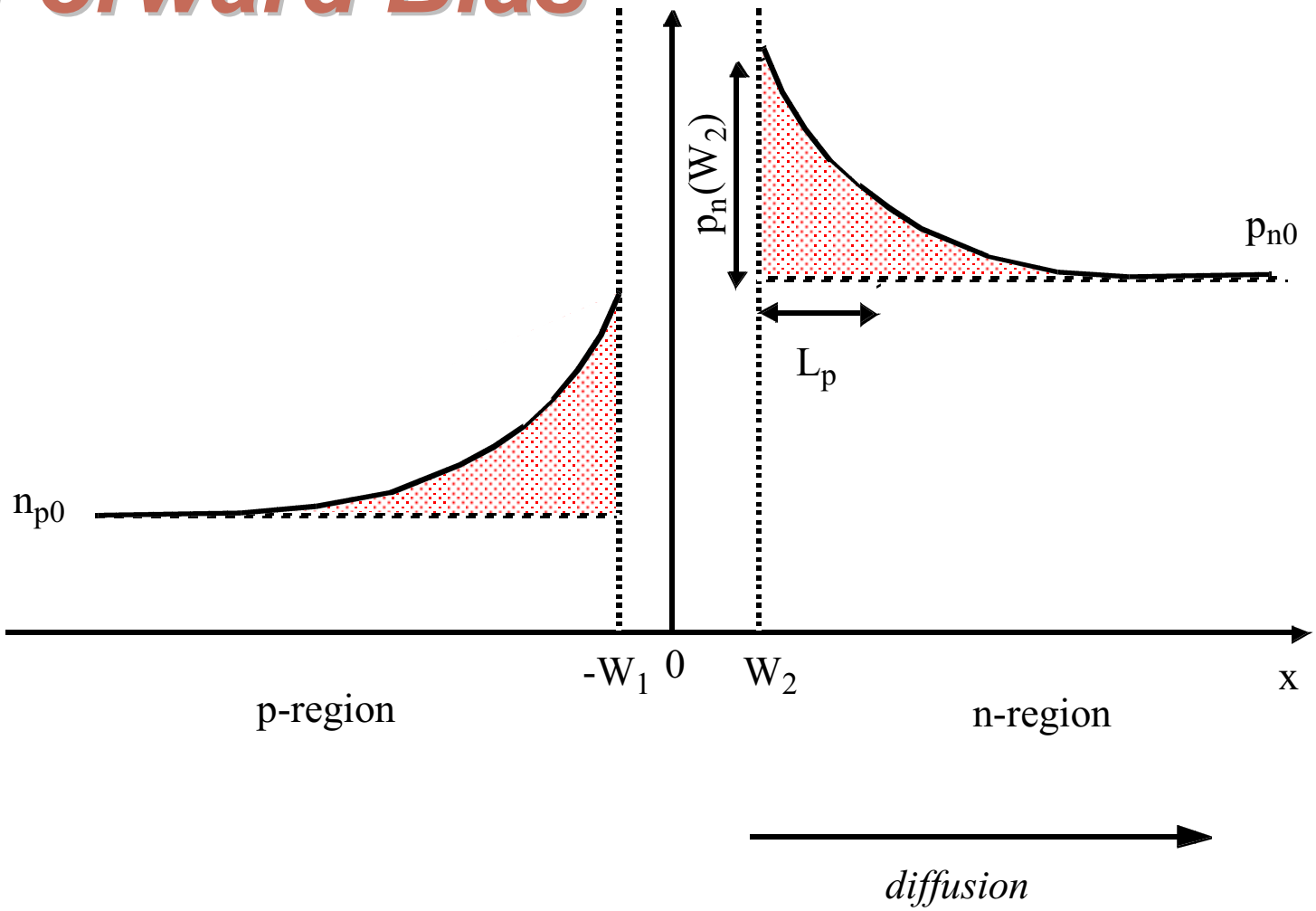
(a) Current flow.

(b) Charge density.

(c) Electric field.

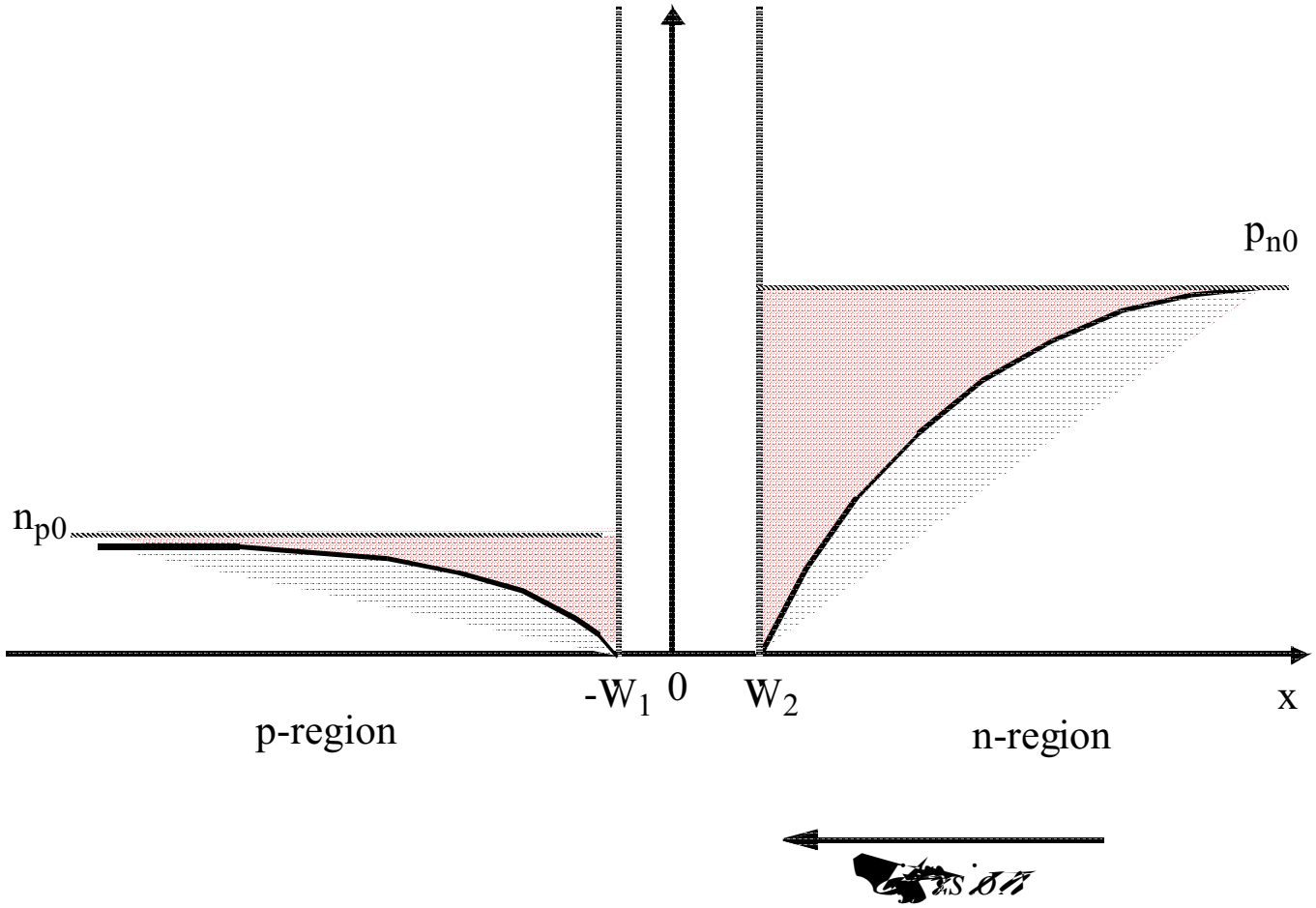
(d) Electrostatic potential.

Forward Bias



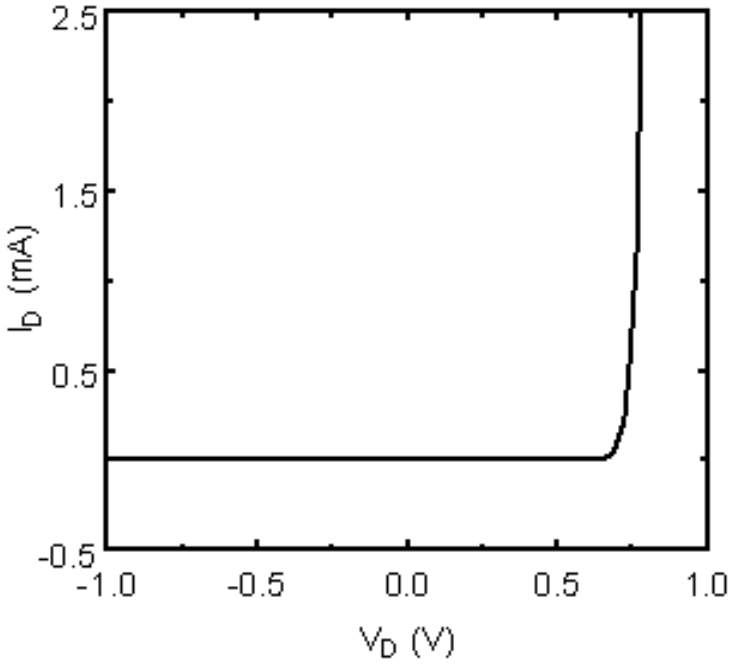
Forward Bias usually avoided in Digital ICs

Reverse Bias

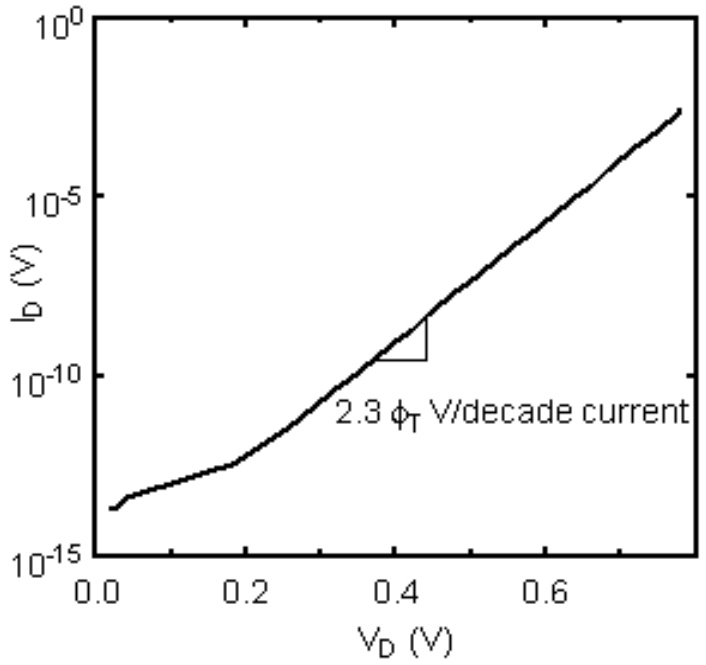


Diode Isolation Mode

Diode Current



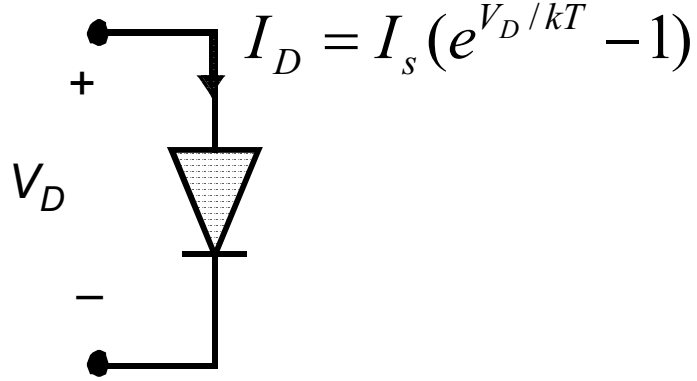
(a) On a linear scale.



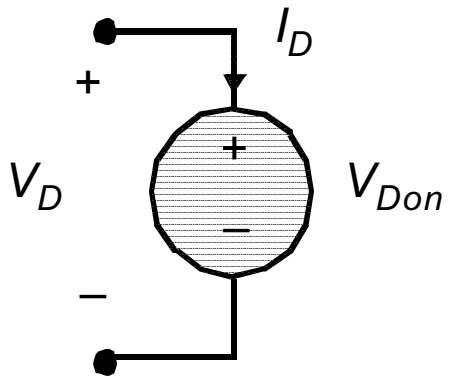
(b) On a logarithmic scale (forward bias).

$$I_D = I_s(e^{V_D/kT} - 1)$$

Models for Manual Analysis

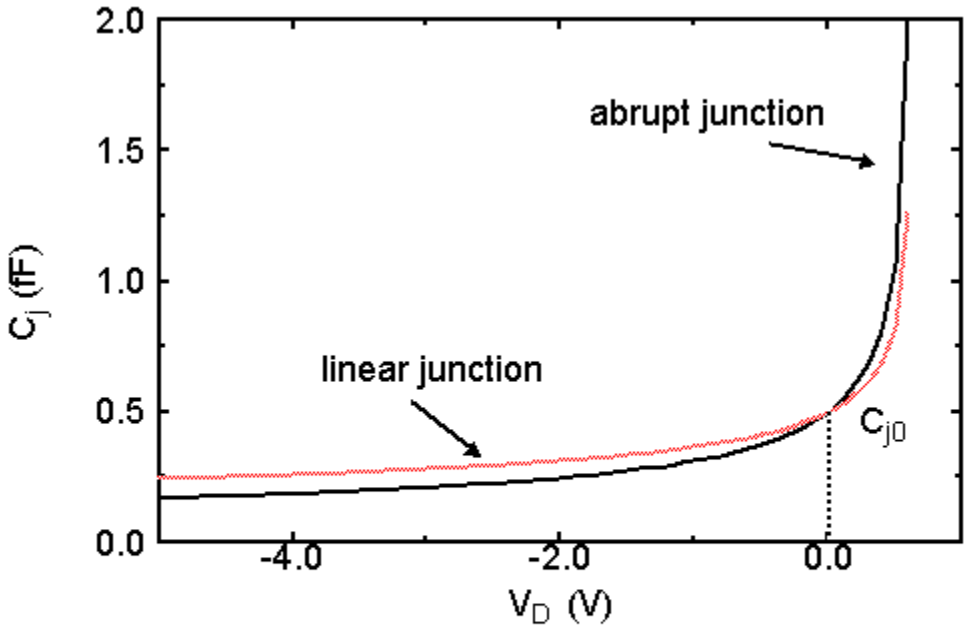


(a) Ideal diode model



(b) First-order diode model

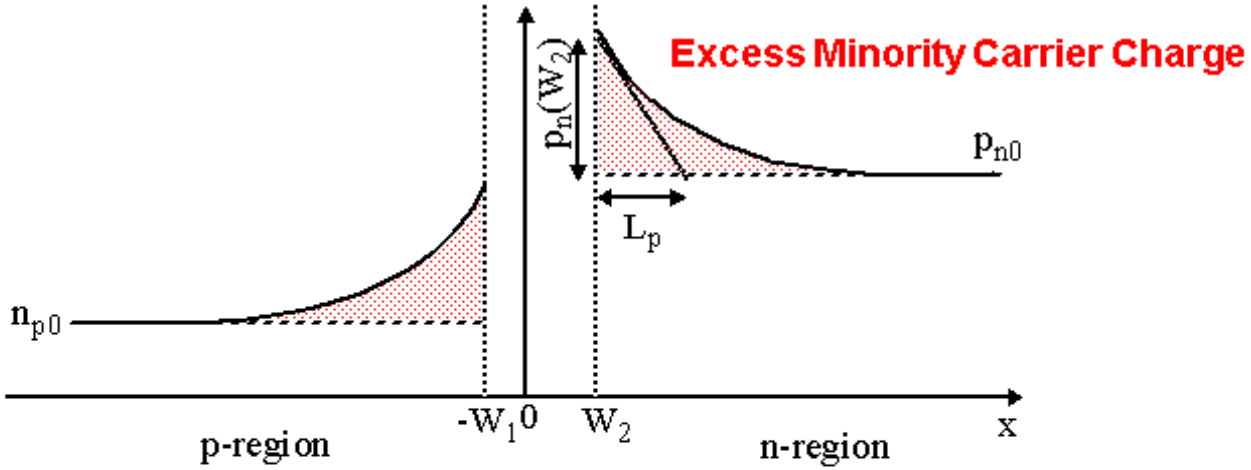
Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

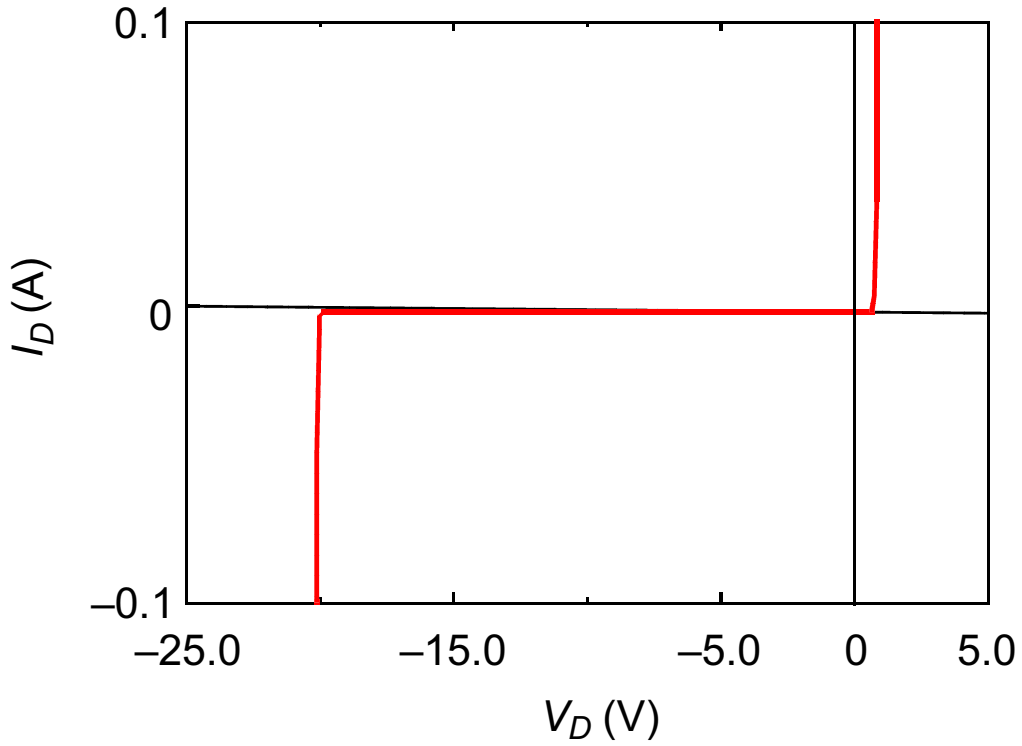
m = 0.5: abrupt junction
m = 0.33: linear junction

Diffusion Capacitance (Forward Bias)



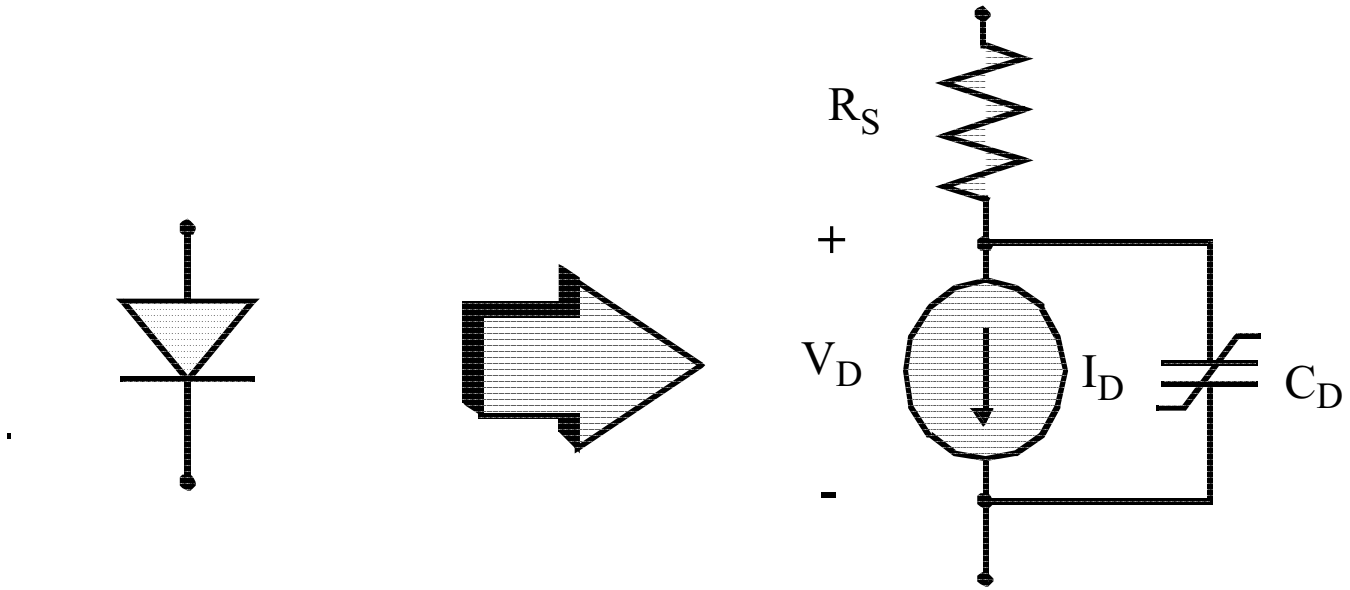
$$C_d = \frac{dQ_D}{dV_D} = \tau_T \frac{dI_D}{dV_D} \approx \frac{\tau_T I_D}{\phi_T}$$

Secondary Effects



Avalanche Breakdown

Diode Model (Manual Analysis)



SPICE Parameters

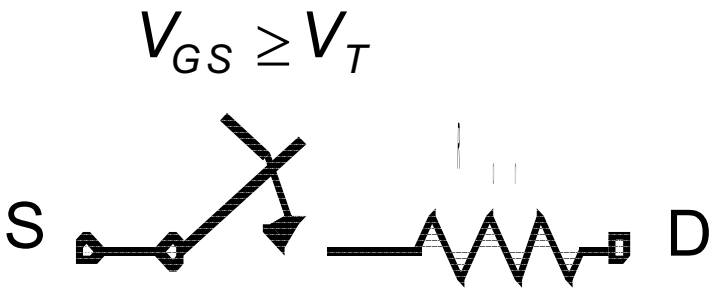
Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

First Order SPICE diode model parameters.

- Transit time models charge storage

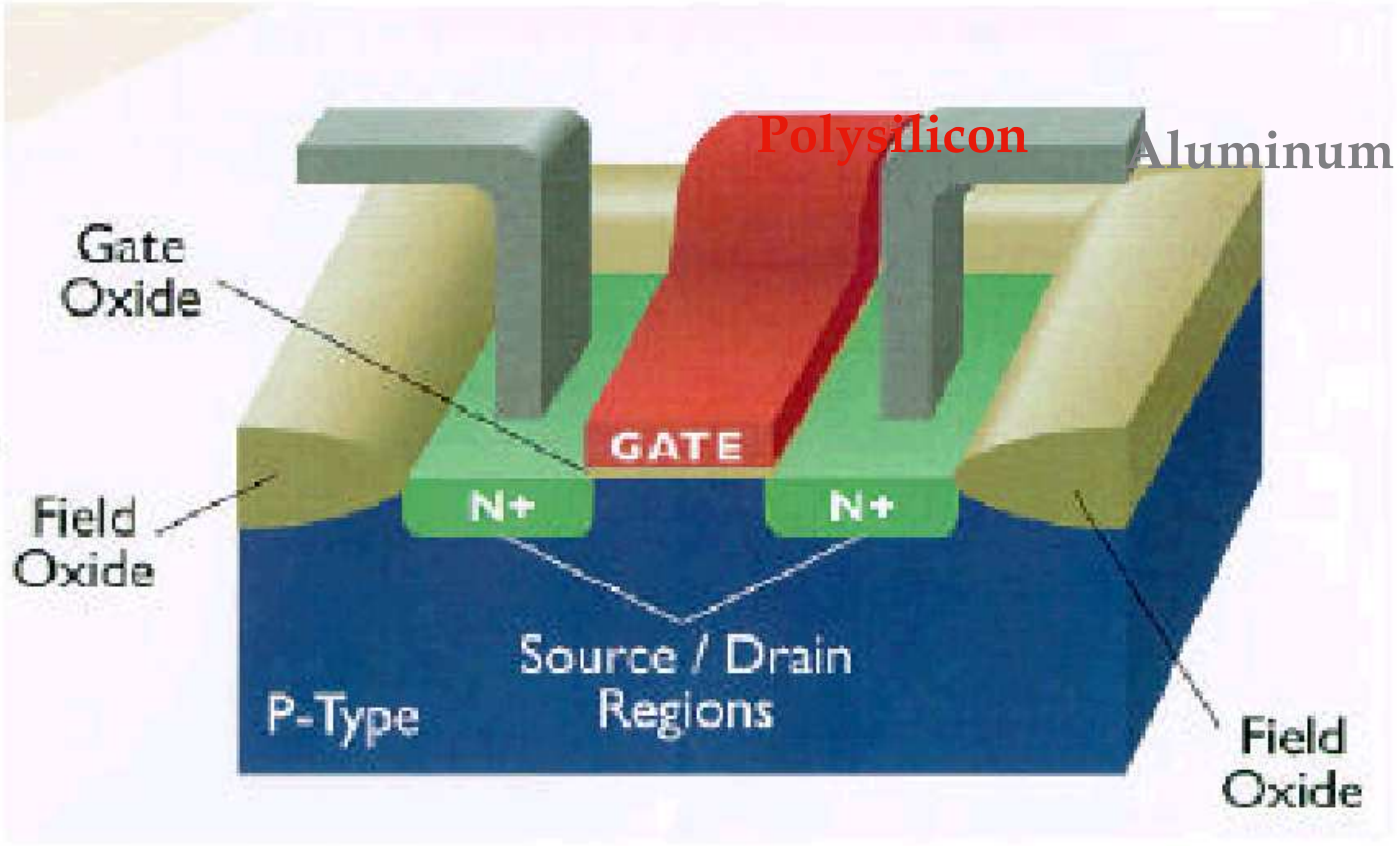
What is a Transistor?

A Switch!

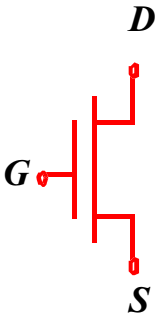


- Resistor is poor model in saturation– current source
- Source and Drain are symmetric
- N-channel: Source is most negative of the two
- P-channel: Source is most positive of the two
- Four Modes:
  - Off (leakage current only)
  - Sub-Threshold (exponential)
  - Linear (Resistive)
  - Saturation (Current Source)

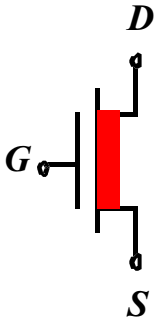
The MOS Transistor



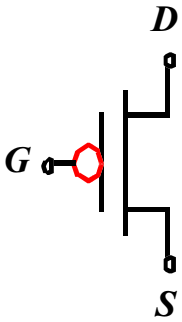
MOS Transistors - Types and Symbols



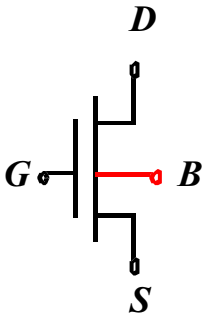
NMOS Enhancement



NMOS Depletion

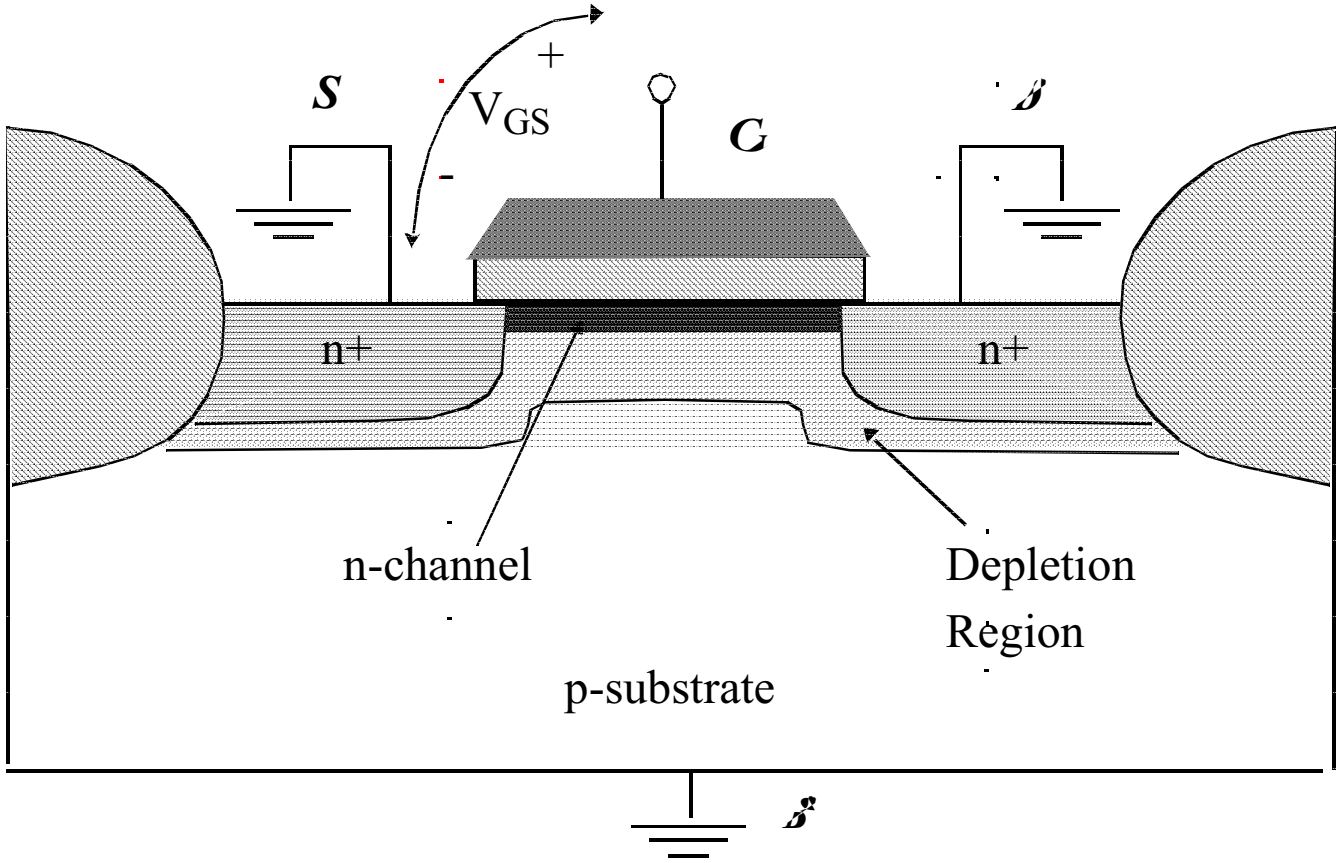


PMOS Enhancement



NMOS with Bulk Contact

Threshold Voltage: Concept



The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference

Depletion Layer Charge

Surface Charge

Implants

Body Effect Coefficient

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

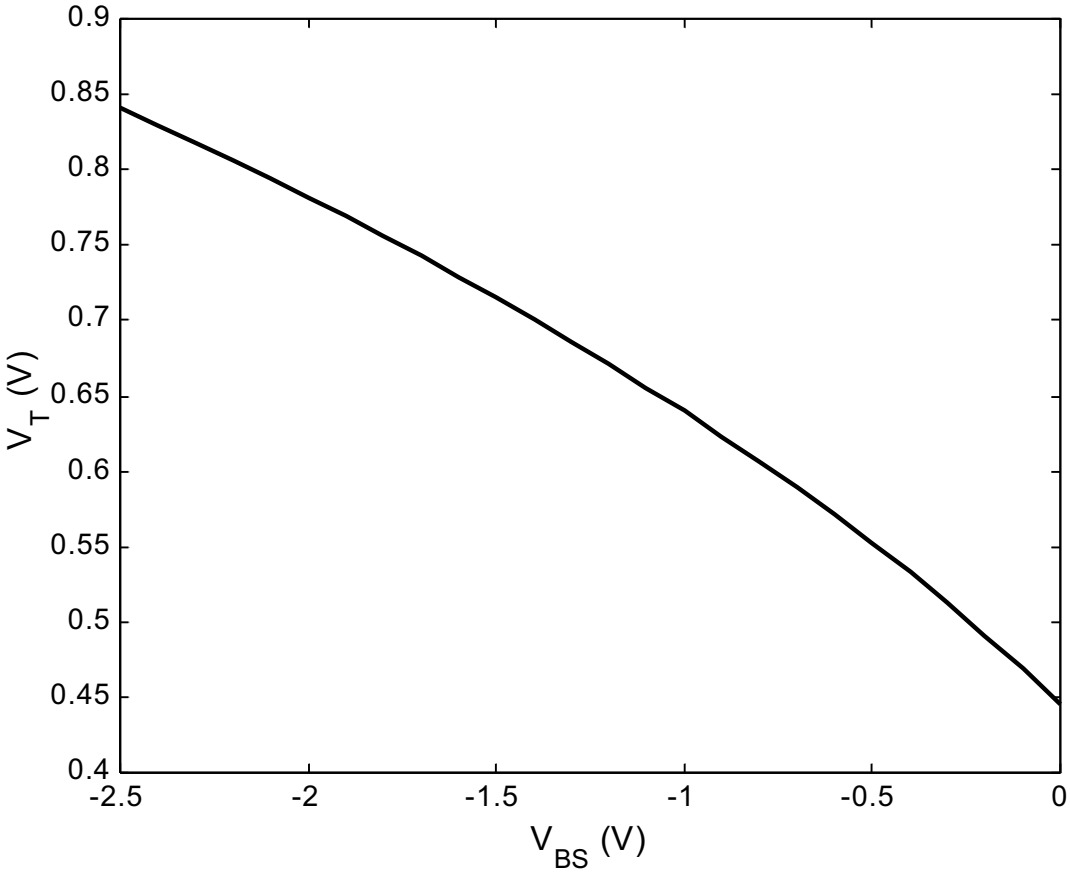
with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

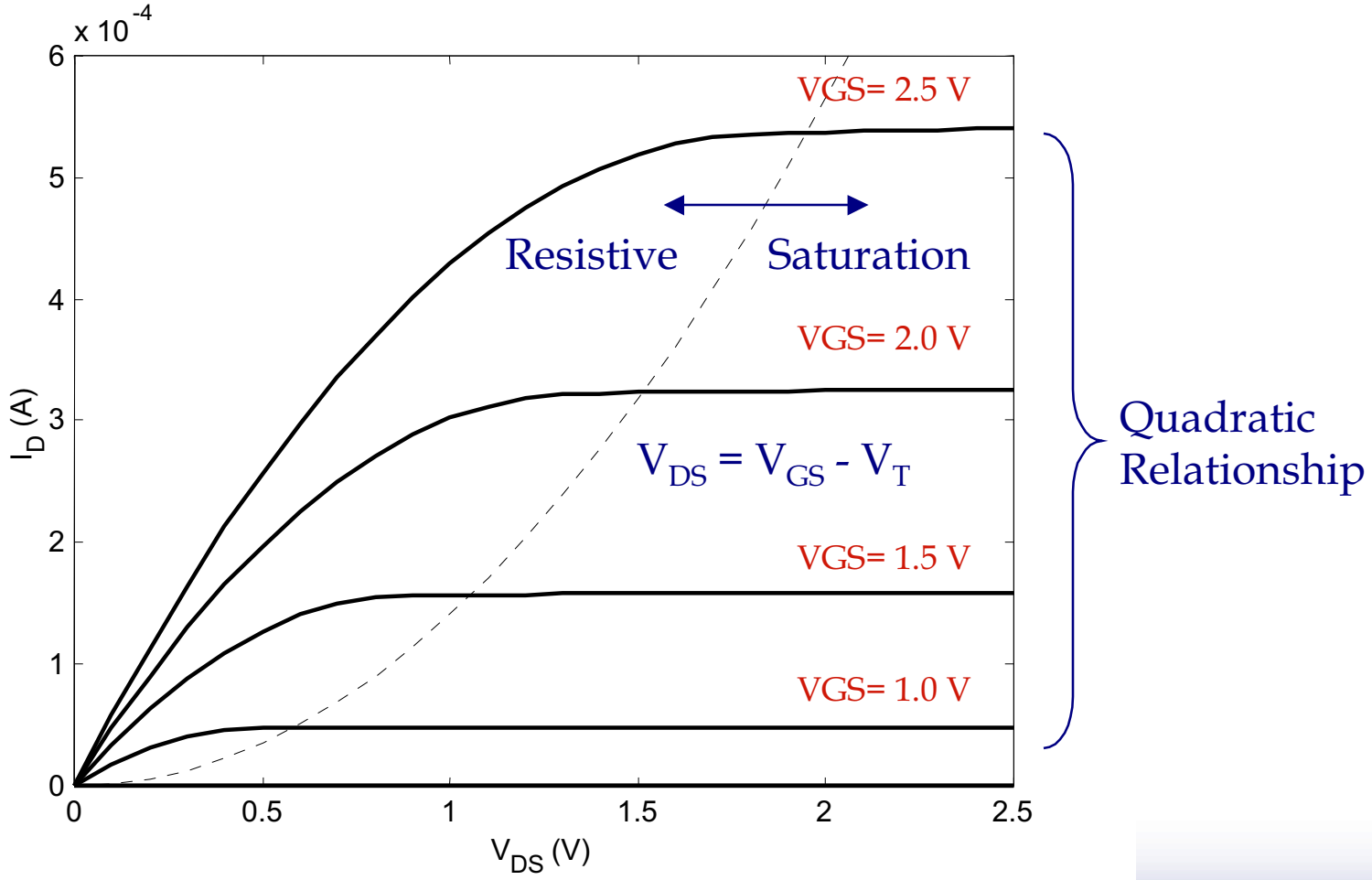
and

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

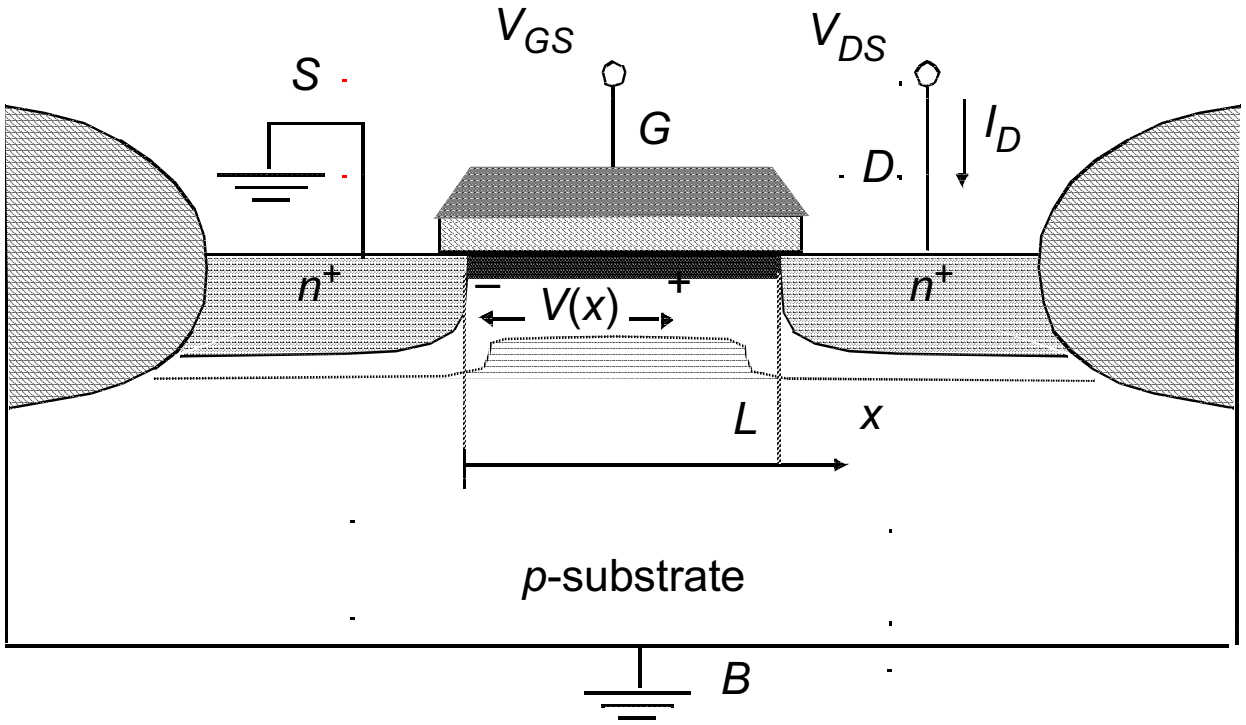
The Body Effect



Current-Voltage Relation

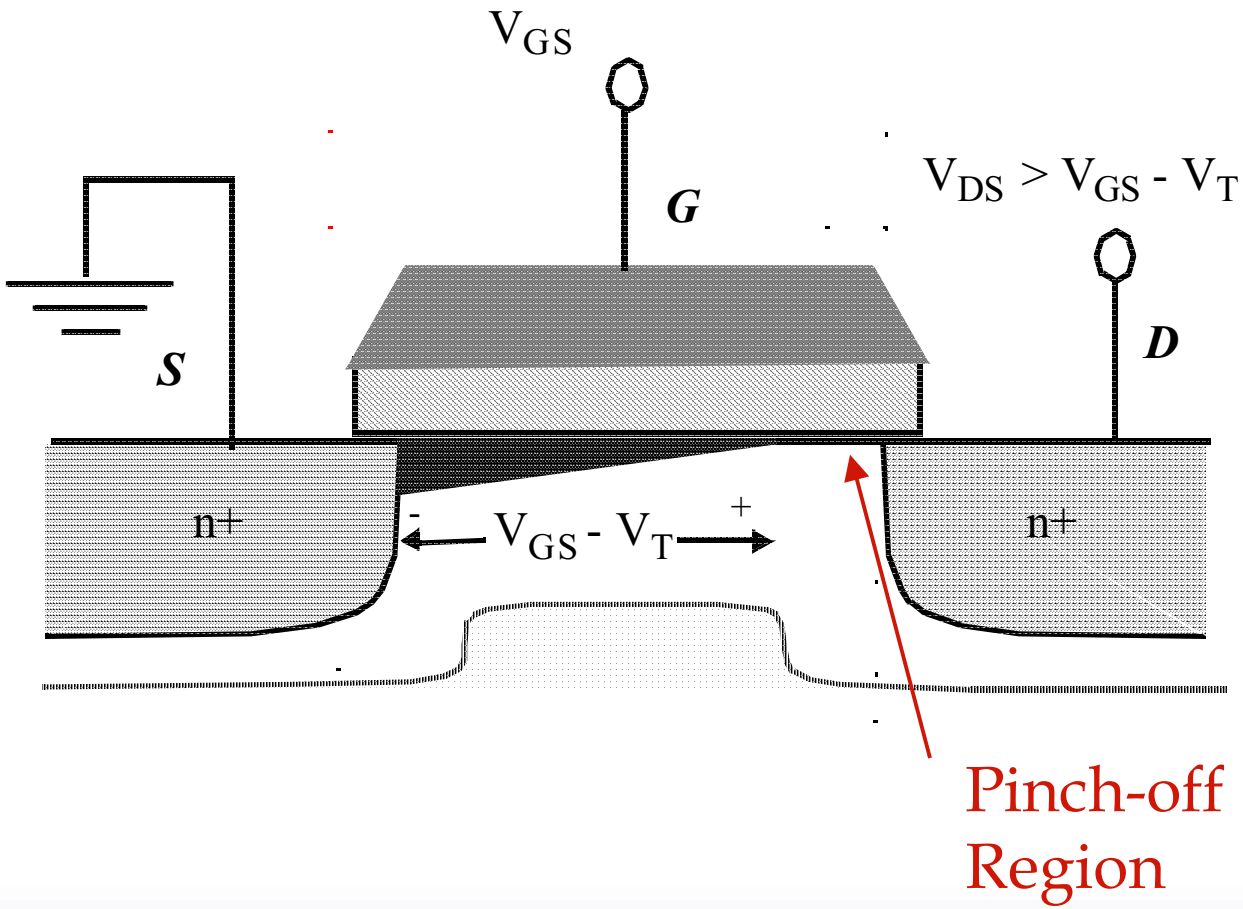


Transistor in Linear



MOS transistor and its bias conditions

Transistor in Saturation



Current-Voltage Relations Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

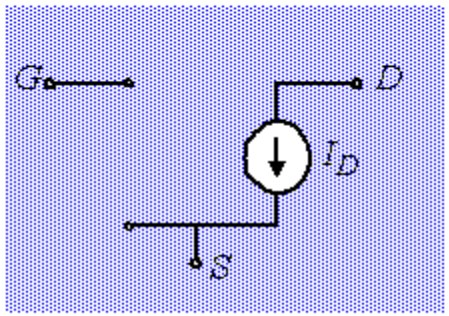
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

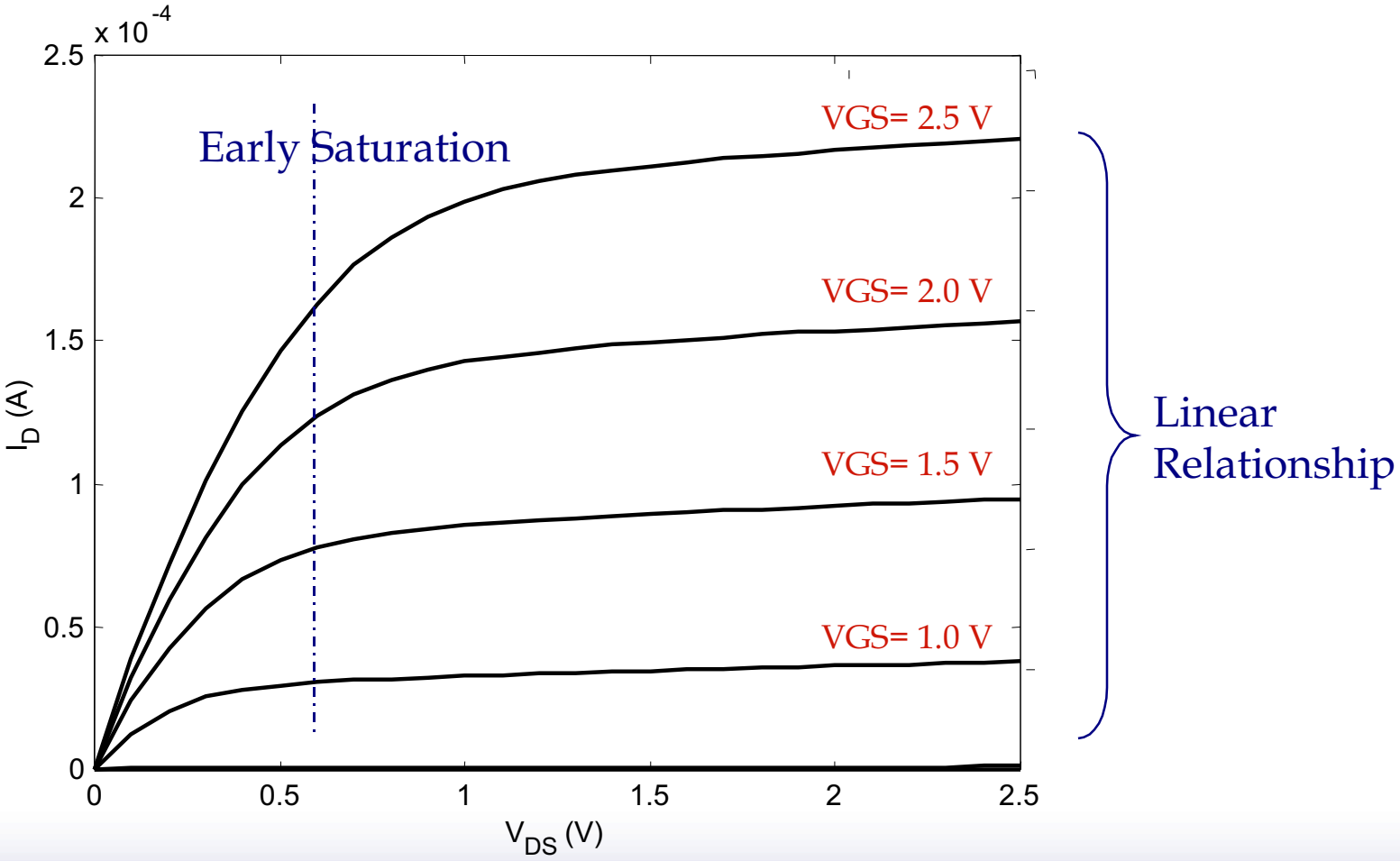
$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

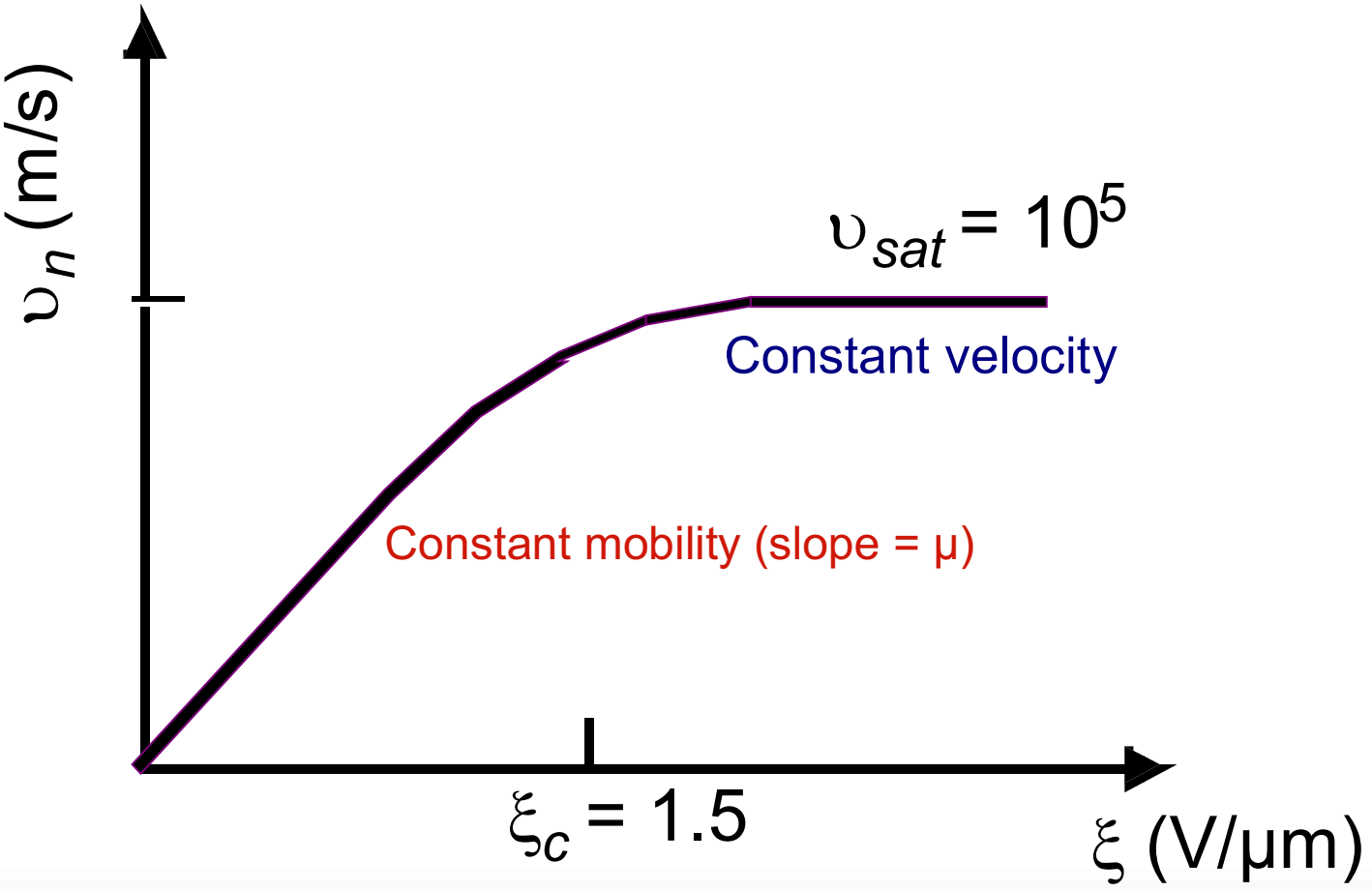
with

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

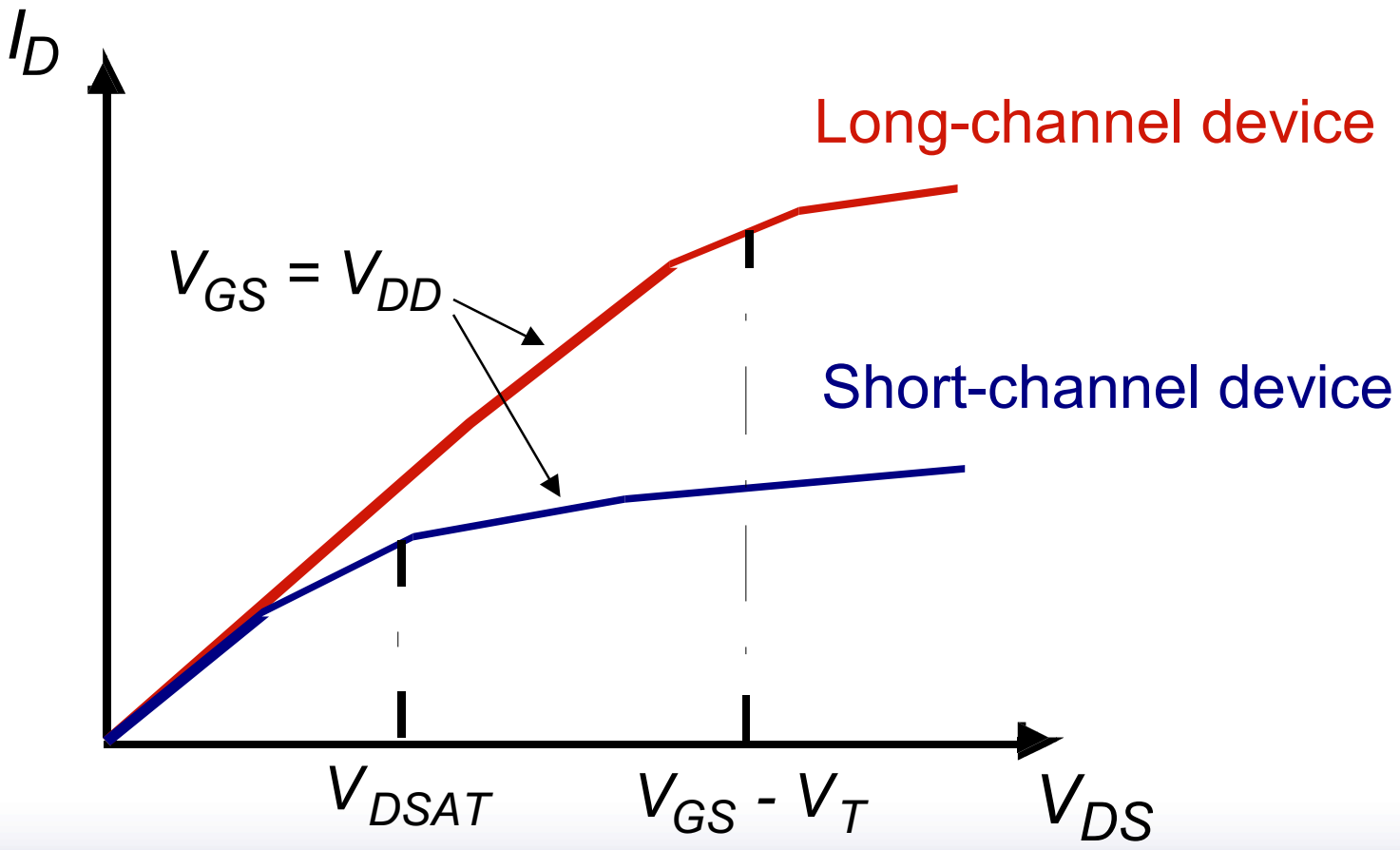
Current-Voltage Relations: Deep-Submicron FET



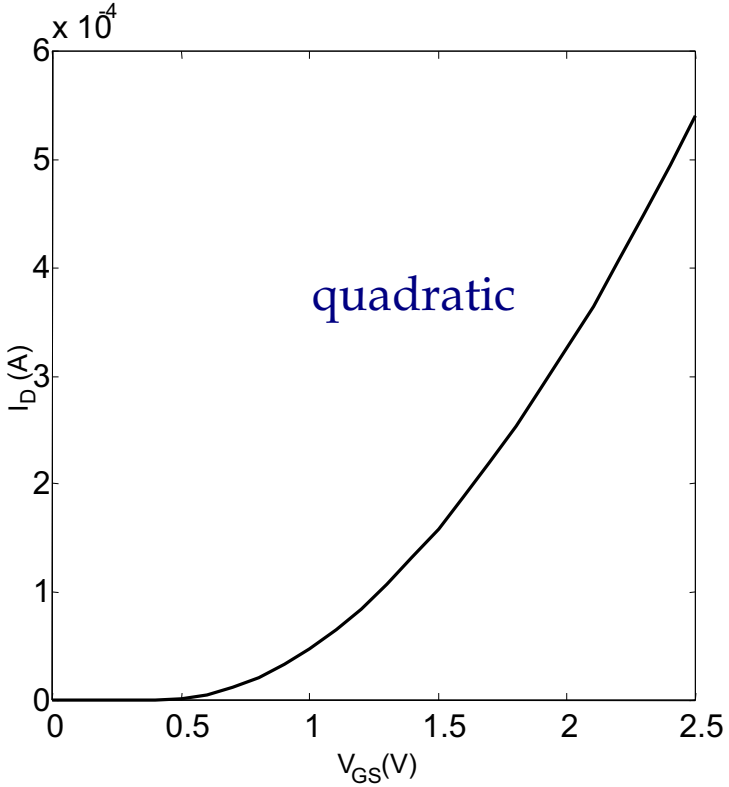
Velocity Saturation



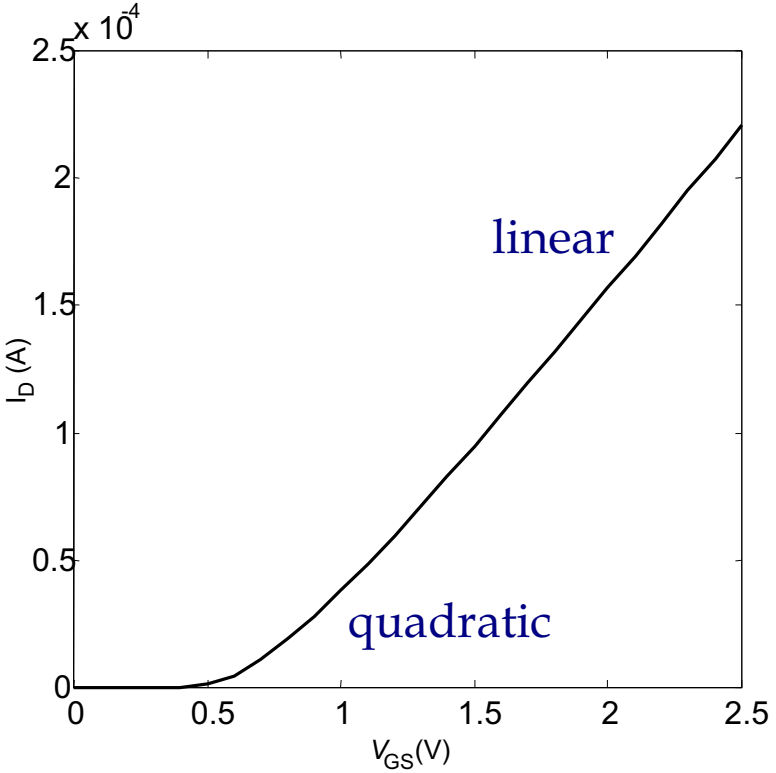
Perspective



I_D versus V_{GS}

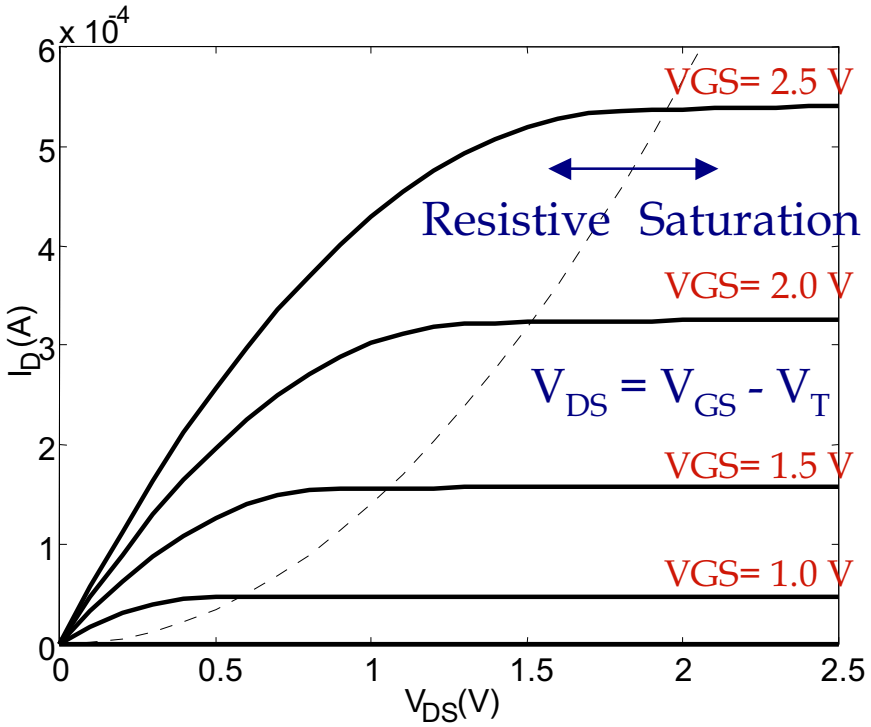


Long Channel

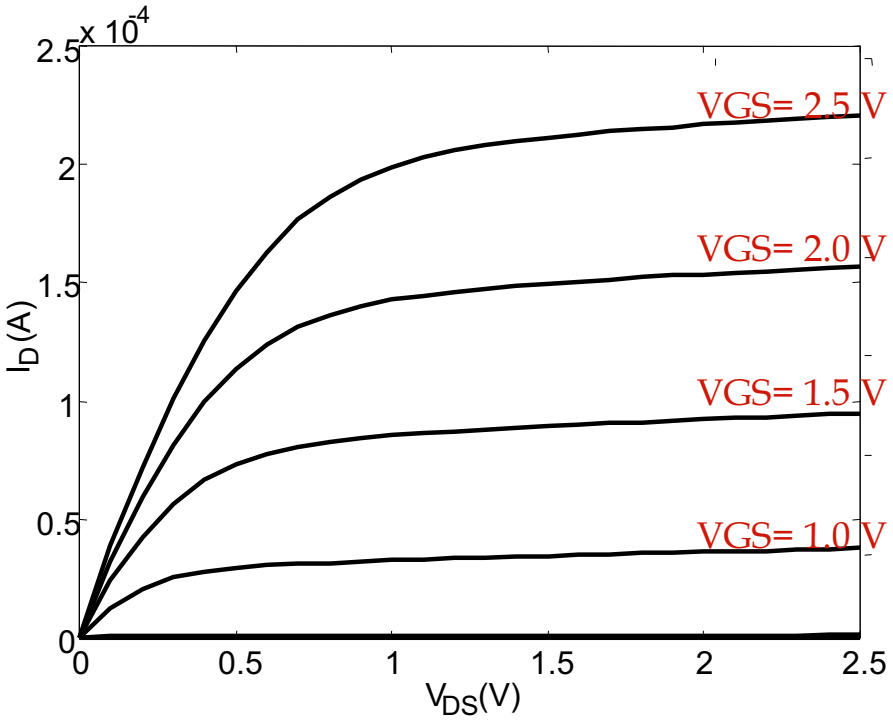


Short Channel

I_D versus V_{DS}

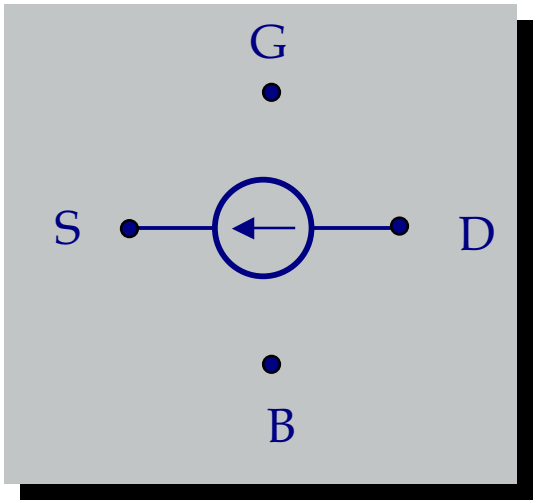


Long Channel



Short Channel

A unified model for manual analysis



$$I_D = 0 \quad \text{for} \quad V_{GT} \le 0$$

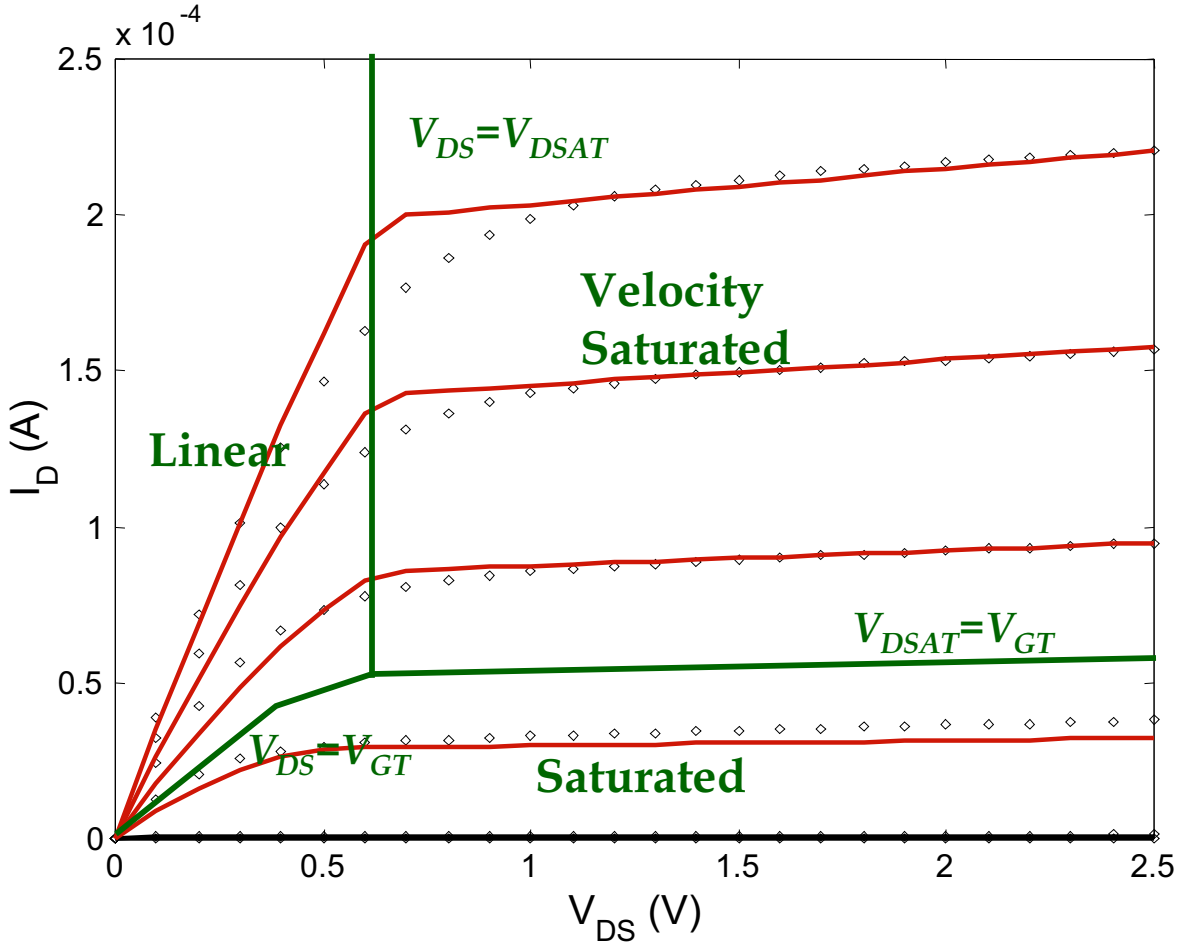
$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \quad \text{for} \quad V_{GT} \ge 0$$

$$\text{with} \quad V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}),$$

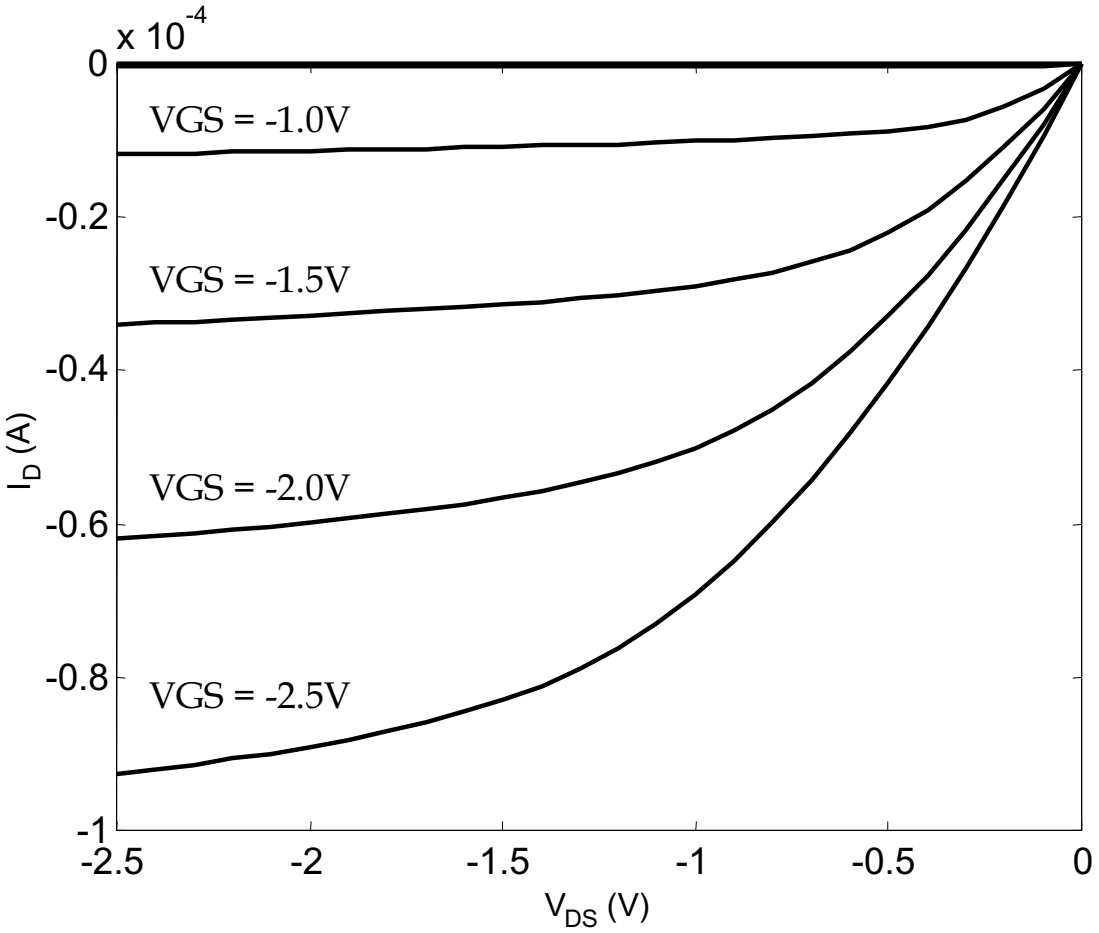
$$V_{GT} = V_{GS} - V_T,$$

$$\text{and} \quad V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

Simple Model versus SPICE



A PMOS Transistor



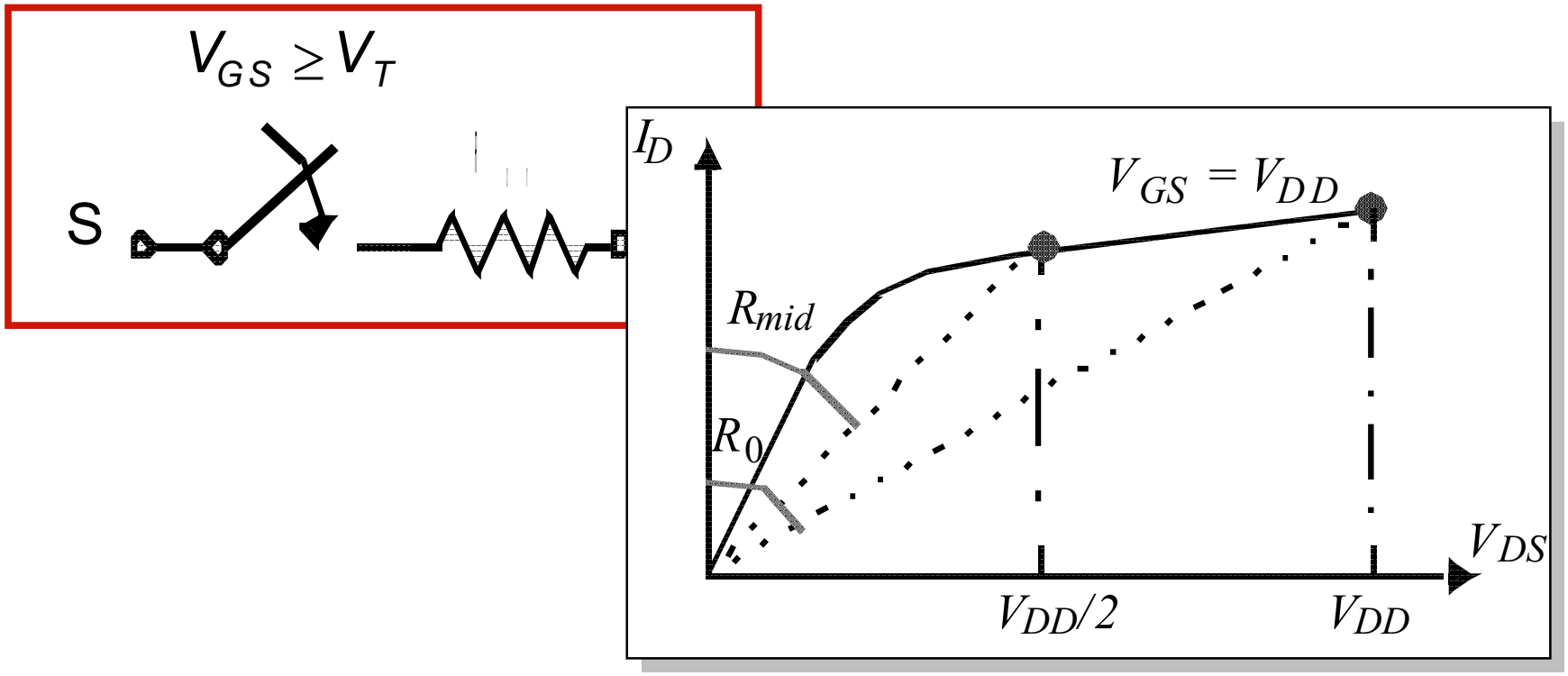
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

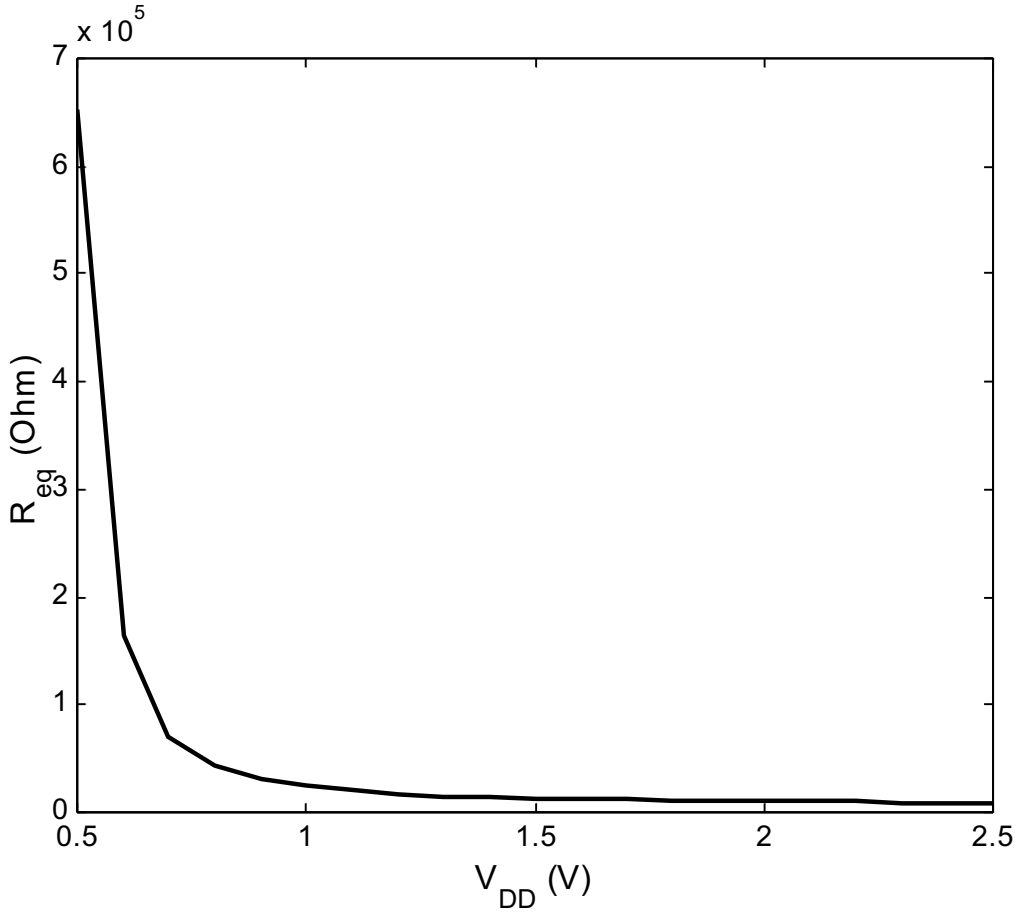
0.5 μm	Vt	Gamma	Vd(sat)	k' (μA/V2)	Lambda
NMOS	0.7-0.8	0.48	3.1	50-60	0.04*
PMOS	-0.91- -0.97	0.59	-6.5	-17- -20	-0.07*

The Transistor as a Switch



$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

The Transistor as a Switch



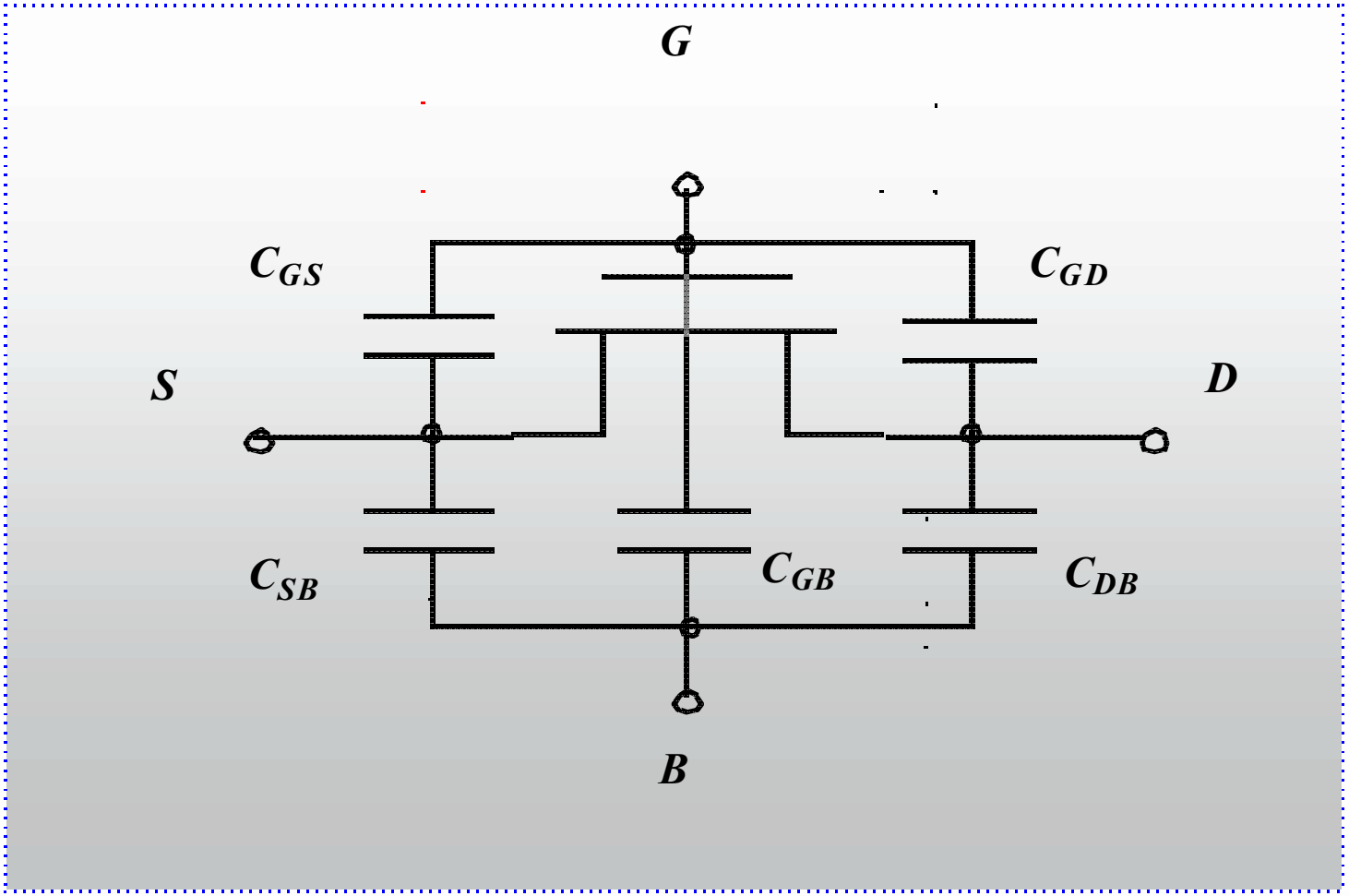
The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

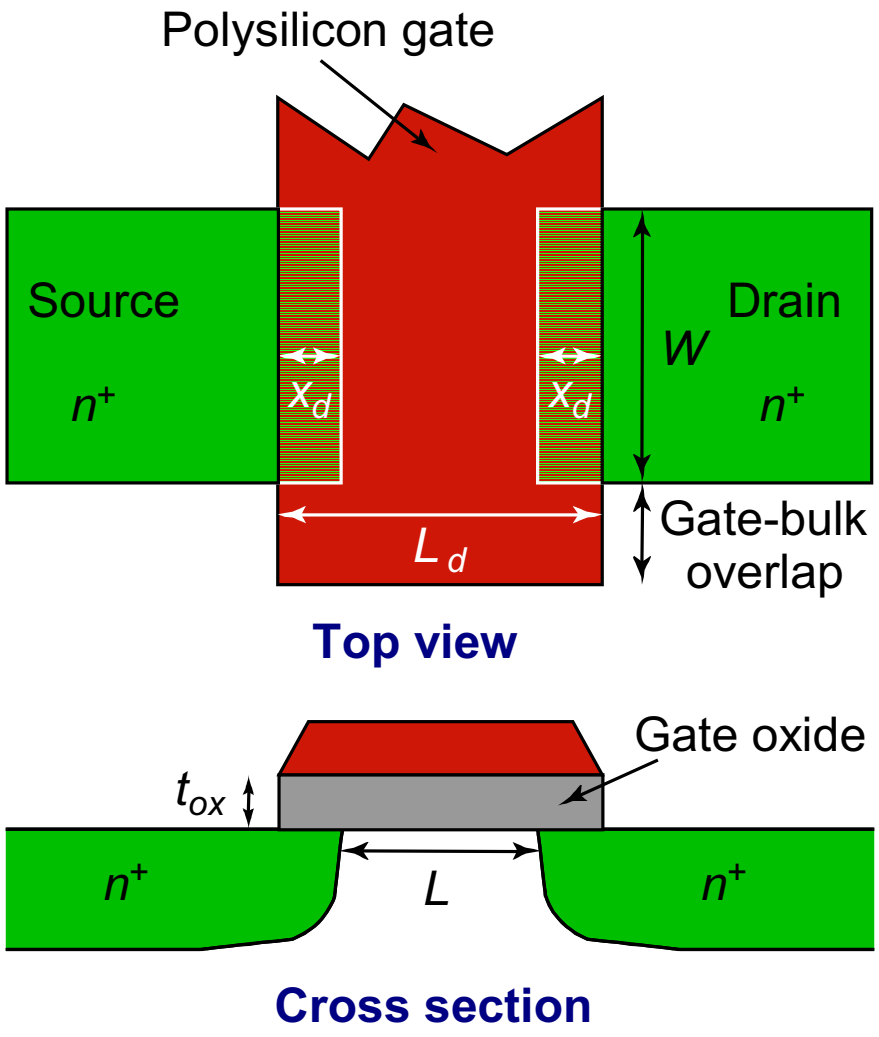
V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

MOS Capacitances
Dynamic Behavior

Dynamic Behavior of MOS Transistor

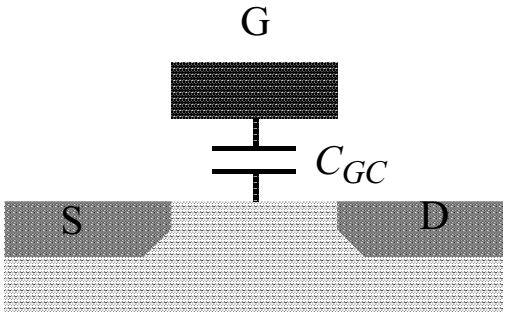


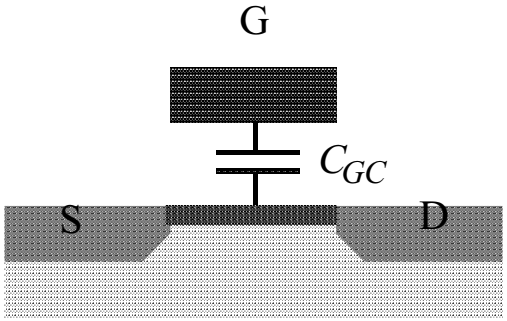
The Gate Capacitance

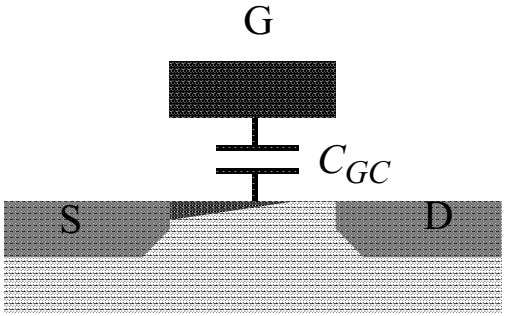


$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

Gate Capacitance



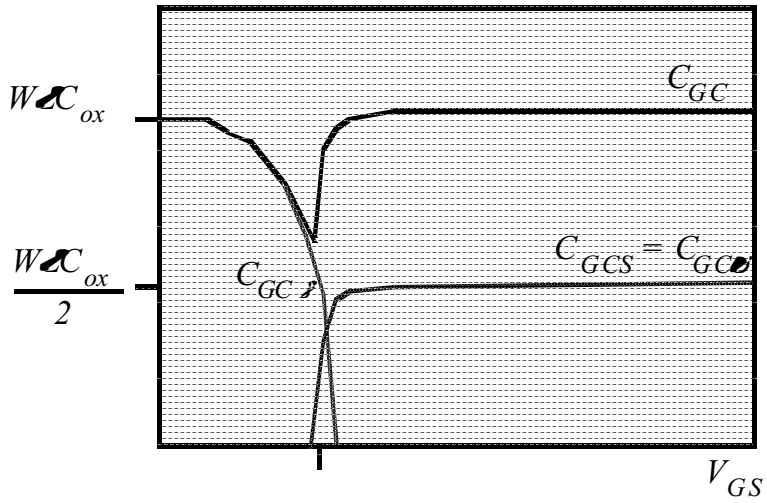




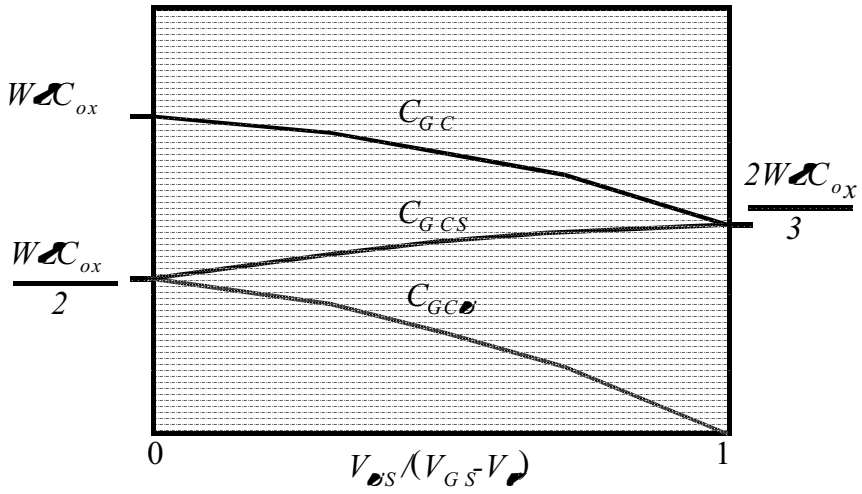
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

Gate Capacitance

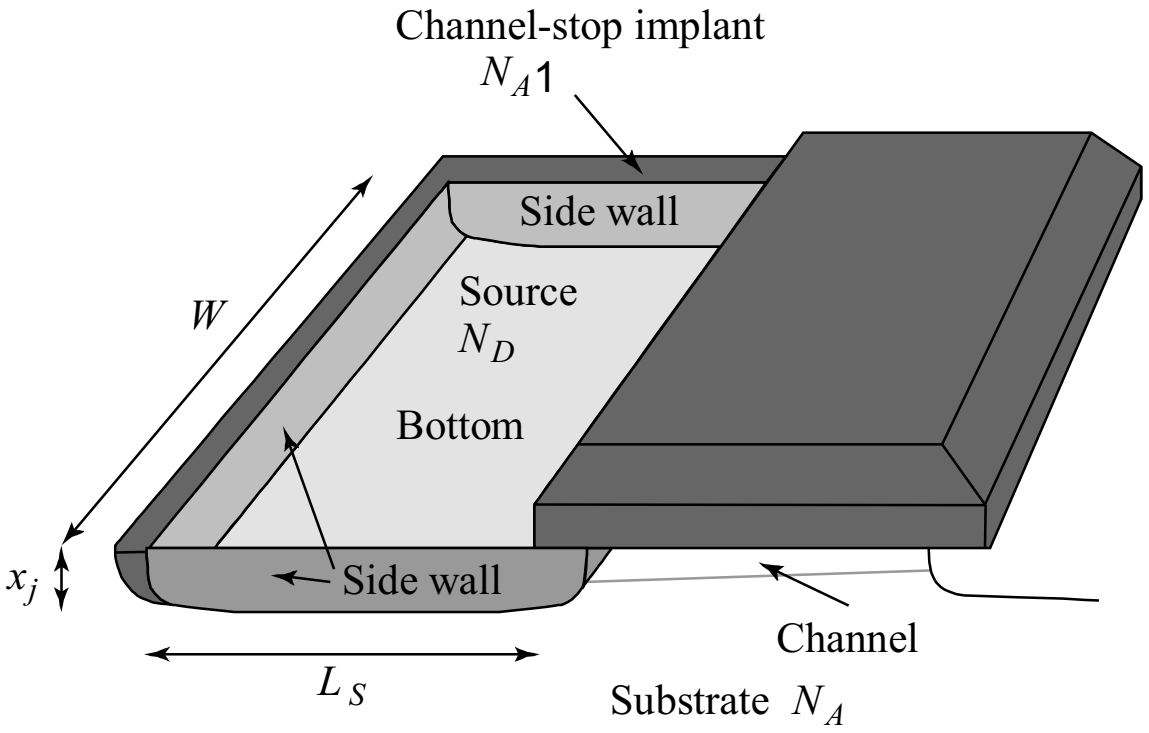


Capacitance as a function of VGS (with VDS = 0)



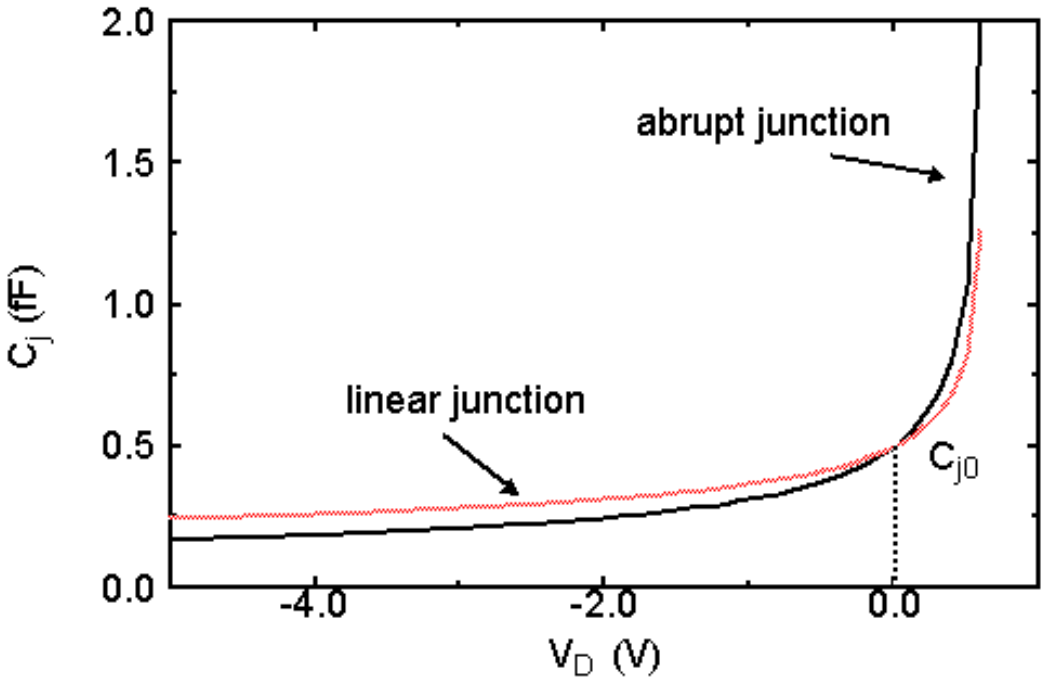
Capacitance as a function of the degree of saturation

Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Capacitances in 0.25/0.5 μm CMOS processes

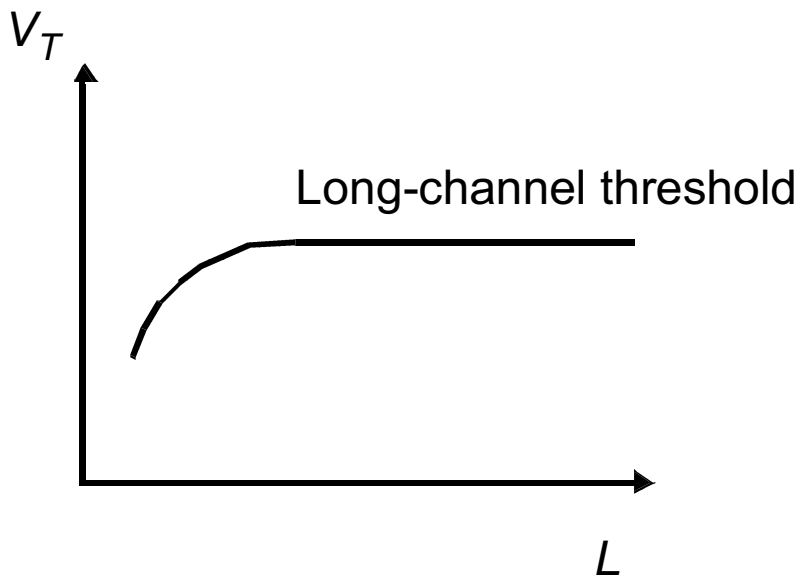
	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_j (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

0.5um AMI/C5	C_{ox} fF/μm^2	C_0 fF/μm	C_j fF/μm^2	m_j	ϕ_b V	C_{jsw} fF/μm	m_{jsw}	ϕ_{bsw} V
NMOS	2.5	0.20	0.44	0.34	0.90	0.28	0.35	0.89
PMOS	2.4	0.28	0.73	0.5	0.91	0.33	0.32	0.90

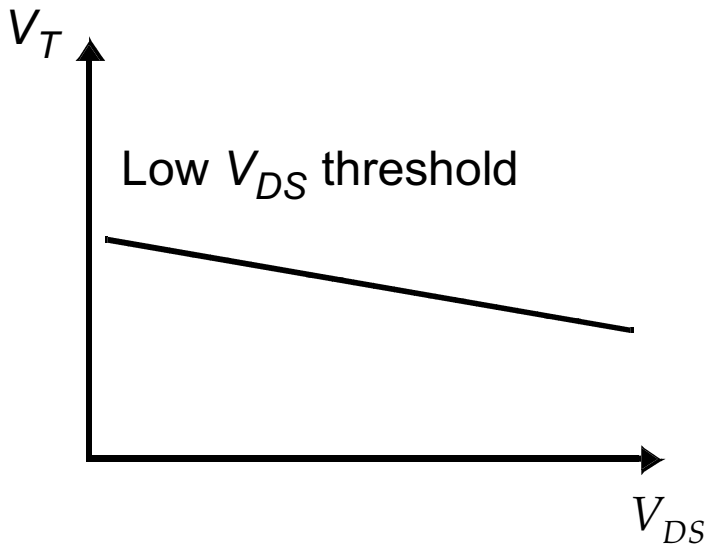
The Sub-Micron MOS Transistor

- Threshold Variations
- Subthreshold Conduction
- Parasitic Resistances

Threshold Variations

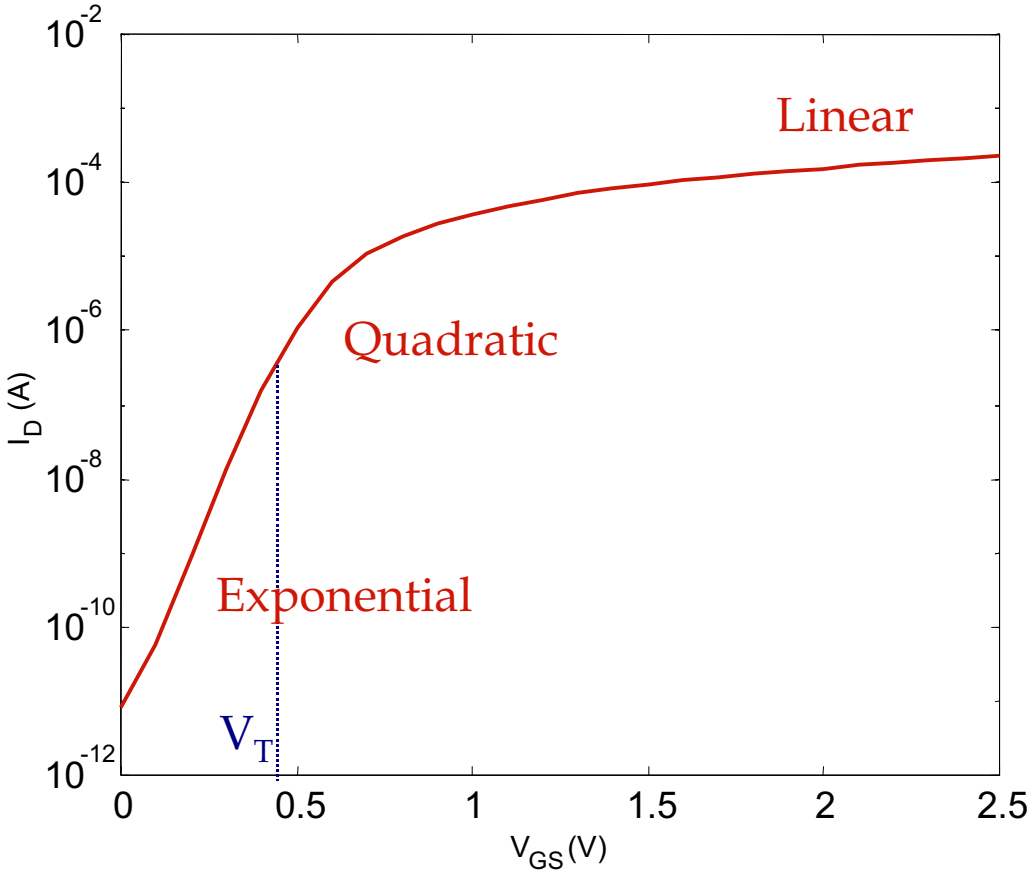


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Sub-Threshold Conduction



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

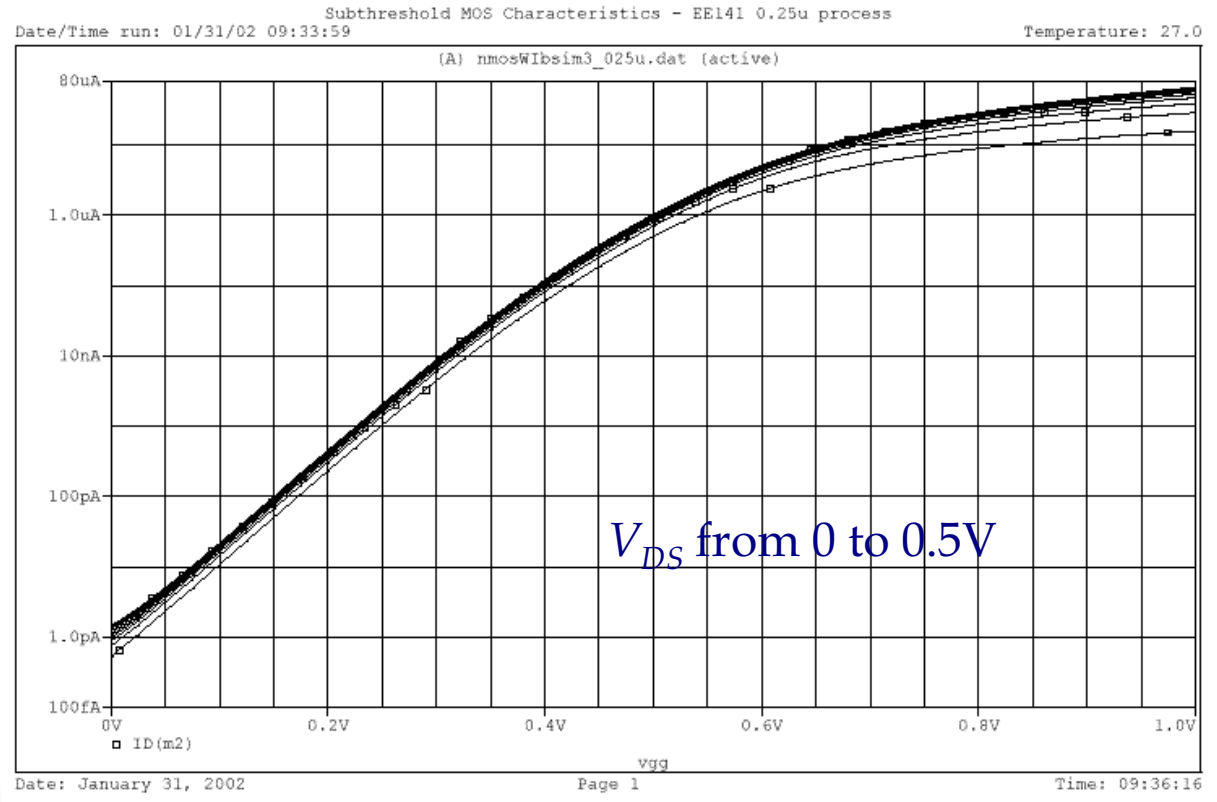
S is ΔV_{GS} for I_{D2}/I_{D1} =10

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

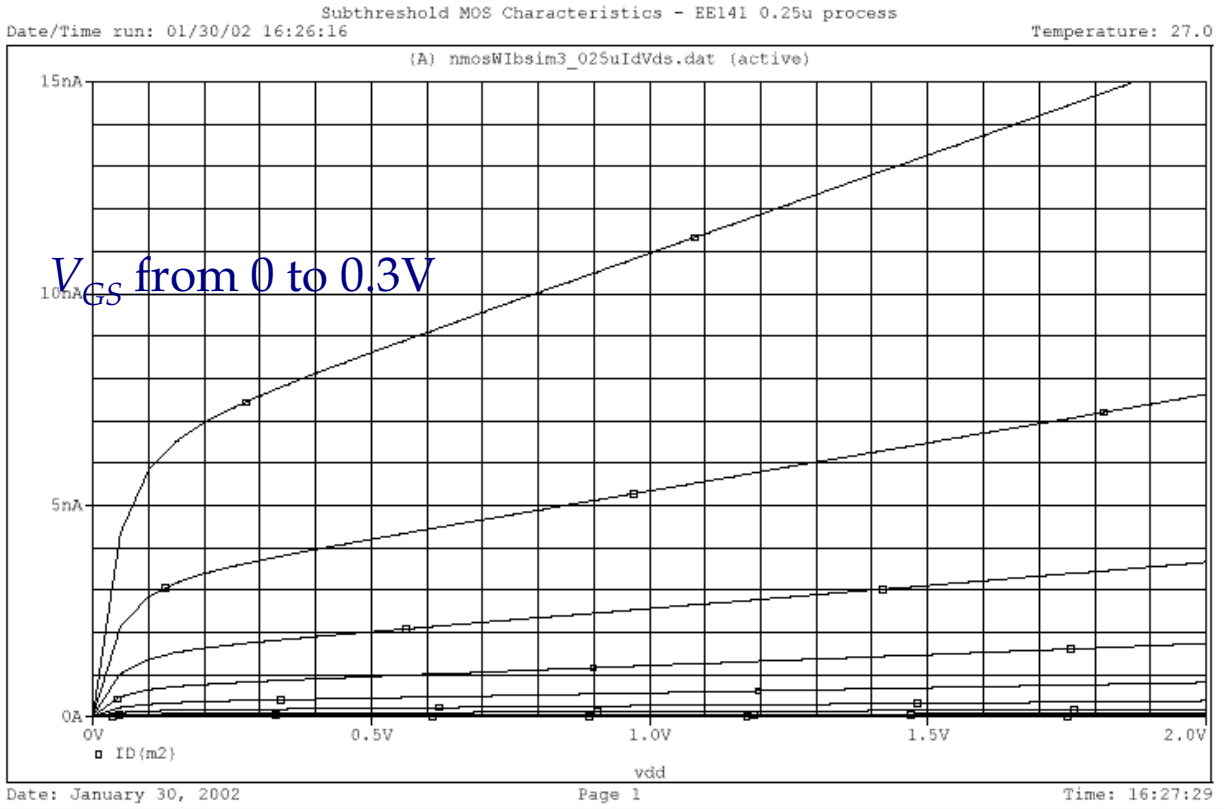
Sub-Threshold I_D vs V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$



Sub-Threshold I_D vs V_{DS}

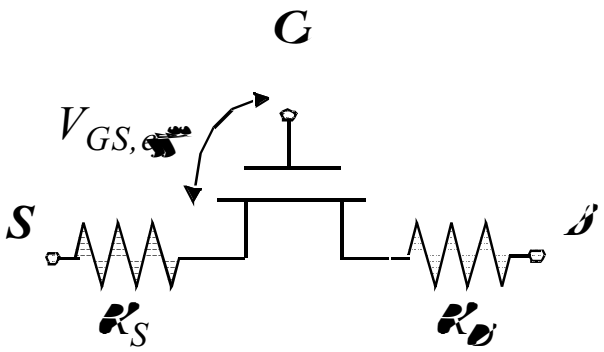
$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) 1 + \lambda \cdot V_{DS}$$

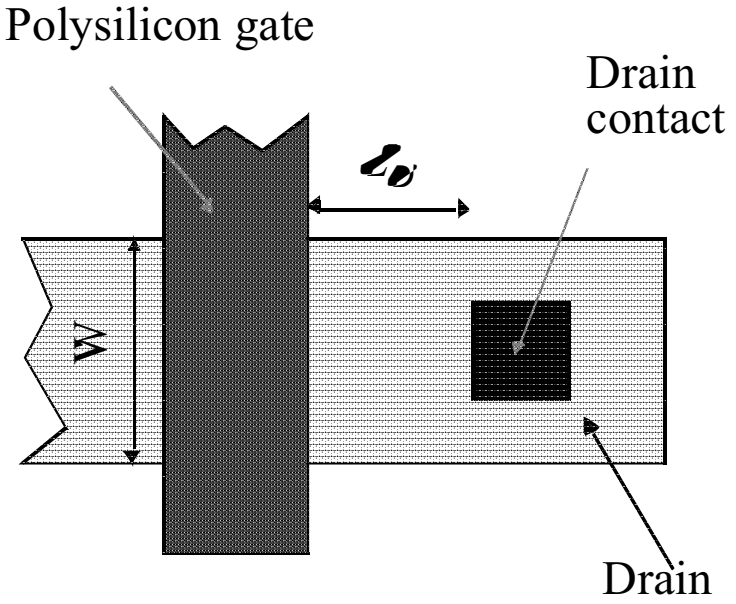


Summary of MOSFET Operating Regions

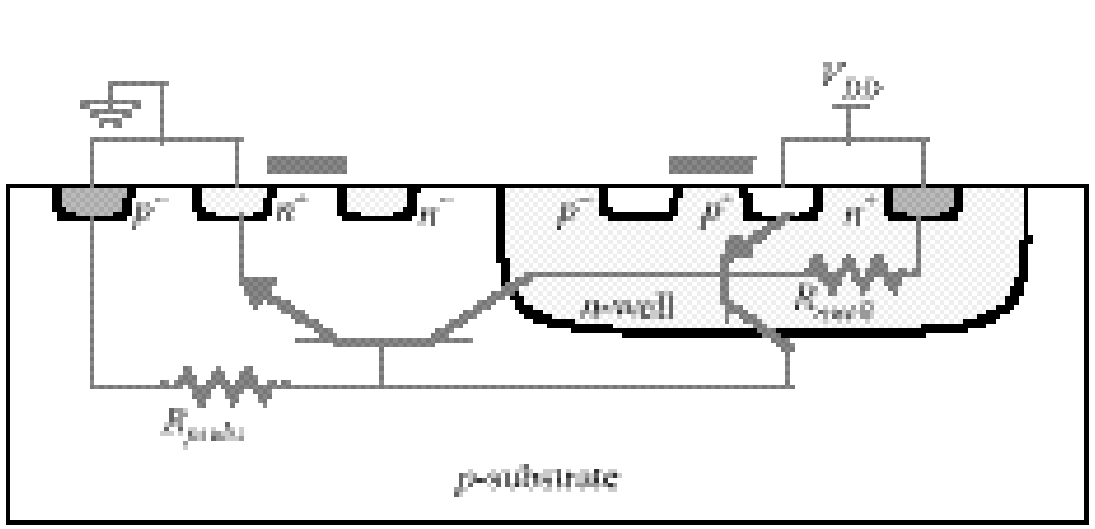
- Strong Inversion $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
  - Exponential in V_{GS} with linear V_{DS} dependence

Parasitic Resistances

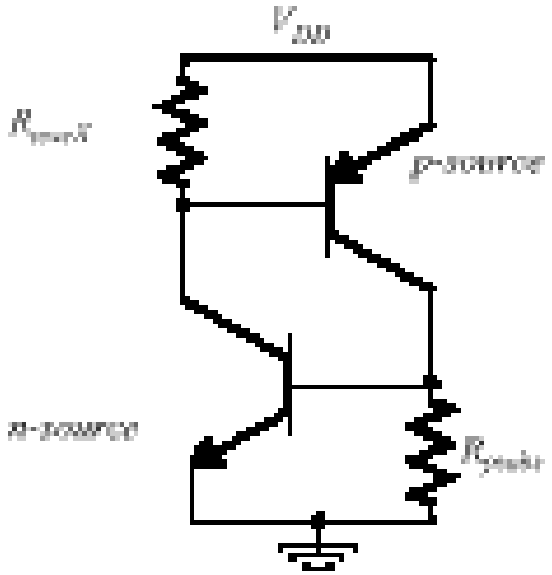




Latch-up

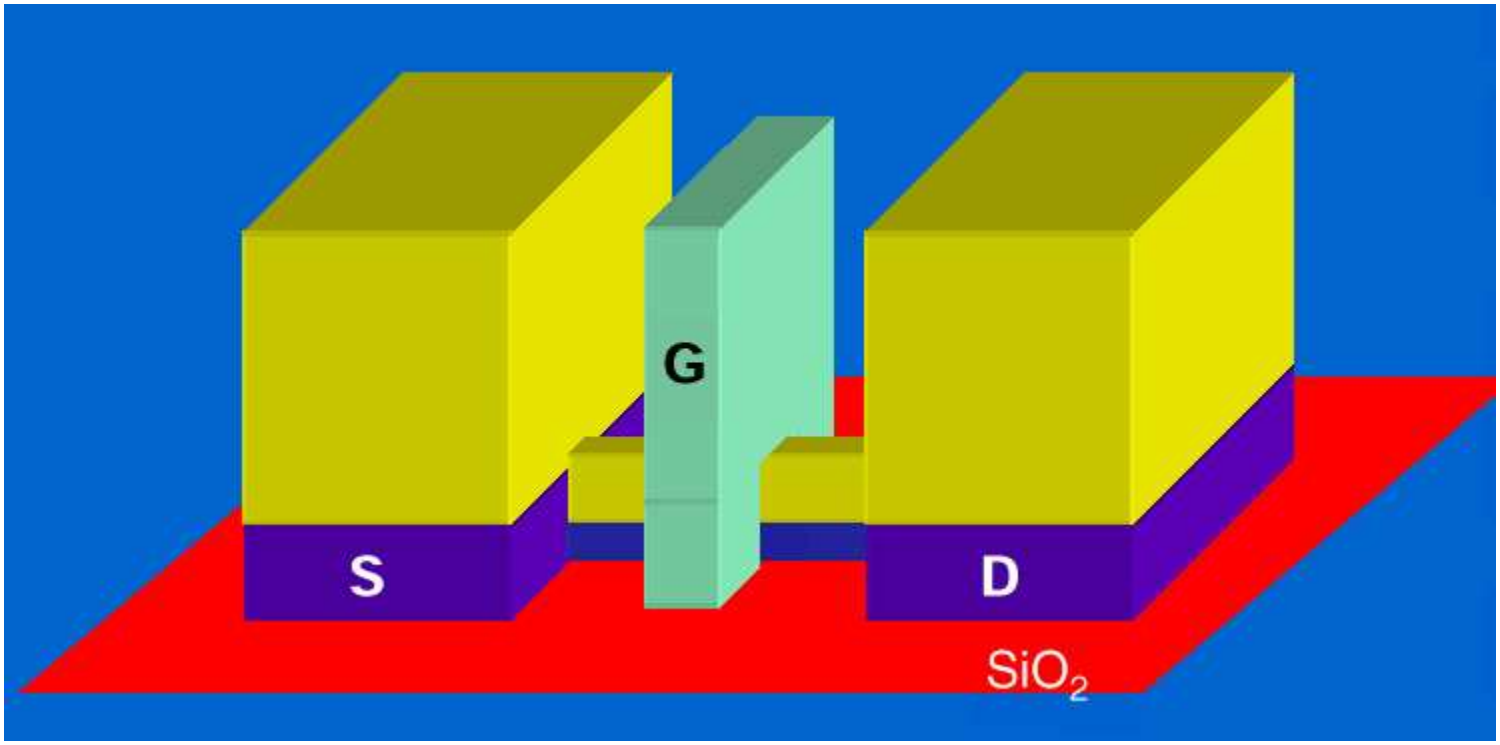


(a) Origin of latchup



(b) Equivalent circuit

Future Perspectives



25 nm FINFET MOS transistor

Problems HW3

1. Rabaey Chap. 3 on-line problems: 2, 3(do not do the spice simulation), 6, 9(L=0.5um)
2. Consider an inverter built with 1/0.5 (nmos W/L) and 2/0.5 (pmos) transistors. Draw a sue schematic for the inverter driving a 10fF load capacitor (other terminal is grounded). Using your model for the AMI FET transistors, determine the peak current flowing into the FET after both an abrupt rising and falling edge on the inverter input, given a supply voltage of 3.3 Volts and using the Mosis extracted parameters from the MOSIS or the class website. Simulate these transitions using spice from the Sue schematic.
3. Complete the Max layout of the full adder cells and build a schematic in sue for each cell and for an 8-bit ripple carry adder. Be sure to use the same transistor sizes in the schematic as you had in your layout. Simulate the adder for the following transition: a=0->1, b=255 Plot the sum and carry outputs and estimate the total carry chain delay and delay per stage.