VLSI Devices

- Intuitive understanding of device operation
- Fundamental analytic models
  - Manual Models
  - Spice Models
- Secondary and deep-sub-micron effects
- Junction Diode and FET
- Resistor and Capacitor
The Diode

Cross-section of \textit{pn} junction in an IC process

One-dimensional representation

\textit{Occurs as parasitic element in Digital ICs}
Depletion Region

(a) Current flow.

(b) Charge density.

(c) Electric field.

(d) Electrostatic potential.
Forward Bias usually avoided in Digital ICs
Reverse Bias

Diode Isolation Mode
**Diode Current**

\[ I_D = I_s \left( e^{V_D/kT} - 1 \right) \]
Models for Manual Analysis

\[ I_D = I_s \left( e^{V_D/kT} - 1 \right) \]

(a) Ideal diode model

(b) First-order diode model
Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\phi_0})^m} \]

- \( m = 0.5 \): abrupt junction
- \( m = 0.33 \): linear junction
**Diffusion Capacitance (Forward Bias)**

Excess Minority Carrier Charge

\[ C_d = \frac{dQ_D}{dV_D} = \tau \frac{dI_D}{I_D} \approx \frac{\tau T \phi_D}{\phi_T} \]
Secondary Effects

Avalanche Breakdown
Diode Model (Manual Analysis)
## SPICE Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation current</td>
<td>$I_S$</td>
<td>IS</td>
<td>A</td>
<td>1.0 E-14</td>
</tr>
<tr>
<td>Emission coefficient</td>
<td>$n$</td>
<td>N</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Series resistance</td>
<td>$R_S$</td>
<td>RS</td>
<td>Ω</td>
<td>0</td>
</tr>
<tr>
<td>Transit time</td>
<td>$\tau_T$</td>
<td>TT</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Zero-bias junction capacitance</td>
<td>$C_{J0}$</td>
<td>CJ0</td>
<td>F</td>
<td>0</td>
</tr>
<tr>
<td>Grading coefficient</td>
<td>$m$</td>
<td>M</td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Junction potential</td>
<td>$\phi_0$</td>
<td>VJ</td>
<td>V</td>
<td>1</td>
</tr>
</tbody>
</table>

First Order SPICE diode model parameters.

- Transit time models charge storage
What is a Transistor?

A Switch!

- Resistor is poor model in saturation—current source
- Source and Drain are symmetric
- N-channel: Source is most negative of the two
- P-channel: Source is most positive of the two
- Four Modes:
  - Off (leakage current only)
  - Sub-Threshold (exponential)
  - Linear (Resistive)
  - Saturation (Current Source)
The MOS Transistor
MOS Transistors - Types and Symbols

NMOS Enhancement

PMOS Enhancement

NMOS Depletion

NMOS with Bulk Contact
Threshold Voltage: Concept
The Threshold Voltage

\[ V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}} \]

Workfunction Difference

Surface Charge

Depletion Layer Charge

Implants

Body Effect Coefficient

\[ V_T = V_{T0} + \gamma \left( \sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|} \right) \]

with

\[ V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}} \]

and

\[ \gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}} \]
The Body Effect
Current-Voltage Relation

\[ V_{DS} = V_{GS} - V_T \]

- Resistive
- Saturation

\[ V_{GS} = 2.5 \text{ V} \]
\[ V_{GS} = 2.0 \text{ V} \]
\[ V_{GS} = 1.5 \text{ V} \]
\[ V_{GS} = 1.0 \text{ V} \]
Transistor in Linear

MOS transistor and its bias conditions
Transistor in Saturation

V_{GS} - V_T

V_{DS} > V_{GS} - V_T

Pinch-off Region
Current-Voltage Relations
Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Channel Length Modulation
A model for manual analysis

\[ V_{DS} > V_{GS} - V_T \]

\[ I_D = \frac{k_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ V_{DS} < V_{GS} - V_T \]

\[ I_D = k_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

with

\[ V_T = V_{T0} + \gamma \left( \sqrt{2 \phi_F + V_{SB}} - \sqrt{-2 \phi_F} \right) \]
Current-Voltage Relations: Deep-Submicron FET
Velocity Saturation

\[ \nu_n (m/s) \]

\[ \nu_{sat} = 10^5 \]

\[ \xi_c = 1.5 \]

\[ \xi (V/\mu m) \]

Constant velocity

Constant mobility (slope = \( \mu \))
Perspective

\[ I_D \]

\[ V_{GS} = V_{DD} \]

Long-channel device

Short-channel device

\[ V_{DSAT} \]

\[ V_{GS} - V_T \]

\[ V_{DS} \]
$I_D$ versus $V_{GS}$

Long Channel

Short Channel

quadratic

linear
$I_D$ versus $V_{DS}$

$V_{DS} = V_{GS} - V_T$

Resistive Saturation

Long Channel

Short Channel

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A unified model for manual analysis

\[ I_D = 0 \quad \text{for} \quad V_{GT} \leq 0 \]

\[ I_D = k' \frac{W}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \quad \text{for} \quad V_{GT} \geq 0 \]

with \( V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) \),

\[ V_{GT} = V_{GS} - V_T, \]

and \( V_T = V_{T0} + \gamma \left( \sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right) \)
Simple Model versus SPICE

\[ I_D (A) \]

\[ V_{DS} = V_{DSAT} \]

Velocity Saturated

Linear

\[ V_{DS} = V_{GT} \]

Saturated

\[ V_{DSAT} = V_{GT} \]
A PMOS Transistor
## Transistor Model for Manual Analysis

### Table 3.2
Parameters for manual model of generic 0.25 µm CMOS process (minimum length device).

<table>
<thead>
<tr>
<th></th>
<th>$V_{T0}$ (V)</th>
<th>$\gamma$ (V$^{0.5}$)</th>
<th>$V_{DSAT}$ (V)</th>
<th>$k'$ (A/V$^2$)</th>
<th>$\lambda$ (V$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$115 \times 10^{-6}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-30 \times 10^{-6}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>0.5 µm</th>
<th>Vt</th>
<th>Gamma</th>
<th>Vd(sat)</th>
<th>$k'$ (µA/V2)</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.7-0.8</td>
<td>0.48</td>
<td>3.1</td>
<td>50-60</td>
<td>0.04*</td>
<td></td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.91- -0.97</td>
<td>0.59</td>
<td>-6.5</td>
<td>-17- -20</td>
<td>-0.07*</td>
<td></td>
</tr>
</tbody>
</table>
The Transistor as a Switch

\[ V_{GS} \geq V_T \]

\[ R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6}\lambda V_{DD}\right) \]
The Transistor as a Switch
The Transistor as a Switch

Table 3.3 Equivalent resistance $R_{eq} (W/L= 1)$ of NMOS and PMOS transistors in 0.25 $\mu$m CMOS process (with $L = L_{min}$). For larger devices, divide $R_{eq}$ by $W/L$.

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (k$\Omega$)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (k$\Omega$)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>
MOS Capacitances
Dynamic Behavior
Dynamic Behavior of MOS Transistor
The Gate Capacitance

\[ C_{\text{gate}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} WL \]

**Polysilicon gate**

**Source**

\( n^+ \)

**Drain**

\( n^+ \)

**Gate-bulk overlap**

**Top view**

**Gate oxide**

**Cross section**

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Gate Capacitance

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>( C_{gb} )</th>
<th>( C_{gs} )</th>
<th>( C_{gd} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>( C_{ox}WL_{eff} )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Triode</td>
<td>0</td>
<td>( C_{ox}WL_{eff}/2 )</td>
<td>( C_{ox}WL_{eff}/2 )</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>( (2/3)C_{ox}WL_{eff} )</td>
<td>0</td>
</tr>
</tbody>
</table>

Most important regions in digital design: saturation and cut-off
Gate Capacitance

Capacitance as a function of VGS (with VDS = 0)

Capacitance as a function of the degree of saturation
Diffusion Capacitance

\[ C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sw}} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER} \]
\[ = C_j L_S W + C_{jsw}(2L_S + W) \]
Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\Phi_0})^m} \]

- \( m = 0.5 \): abrupt junction
- \( m = 0.33 \): linear junction
Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

\[ C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{\text{high}}) - Q_j(V_{\text{low}})}{V_{\text{high}} - V_{\text{low}}} = K_{eq} C_{j0} \]

\[ K_{eq} = \frac{-\phi_0^m}{(V_{\text{high}} - V_{\text{low}})(1 - m)} \left[ (\phi_0 - V_{\text{high}})^{1-m} - (\phi_0 - V_{\text{low}})^{1-m} \right] \]
## MOS Capacitances in 0.25/0.5 μm CMOS processes

<table>
<thead>
<tr>
<th></th>
<th>$C_{ox}$ (fF/μm$^2$)</th>
<th>$C_0$ (fF/μm)</th>
<th>$C_j$ (fF/μm$^2$)</th>
<th>$m_j$</th>
<th>$\Phi_b$ (V)</th>
<th>$C_{jsw}$ (fF/μm)</th>
<th>$m_{jsw}$</th>
<th>$\Phi_{bsw}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>0.5μm AMI/C5</th>
<th>$C_{ox}$ fF/μm$^2$</th>
<th>$C_0$ fF/μm</th>
<th>$C_j$ fF/μm$^2$</th>
<th>$m_j$</th>
<th>$\Phi_b$ V</th>
<th>$C_{jsw}$ fF/μm</th>
<th>$m_{jsw}$</th>
<th>$\Phi_{bsw}$ V</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>2.5</td>
<td>0.20</td>
<td>0.44</td>
<td>0.34</td>
<td>0.90</td>
<td>0.28</td>
<td>0.35</td>
<td>0.89</td>
</tr>
<tr>
<td>PMOS</td>
<td>2.4</td>
<td>0.28</td>
<td>0.73</td>
<td>0.5</td>
<td>0.91</td>
<td>0.33</td>
<td>0.32</td>
<td>0.90</td>
</tr>
</tbody>
</table>
The Sub-Micron MOS Transistor

- Threshold Variations
- Subthreshold Conduction
- Parasitic Resistances
**Threshold Variations**

- **Long-channel threshold**
  - Threshold as a function of the length (for low $V_{DS}$)

- **Low $V_{DS}$ threshold**
  - Drain-induced barrier lowering (for low $L$)
Sub-Threshold Conduction

The Slope Factor

\[ I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}} \]

\( S \) is \( \Delta V_{GS} \) for \( I_{D2}/I_{D1} = 10 \)

\[ S = n \left( \frac{kT}{q} \right) \ln(10) \]

Typical values for \( S \):
60 .. 100 mV/decade
**Sub-Threshold** $I_D$ vs $V_{GS}$

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{\frac{-qV_{DS}}{kT}}\right)$$
Sub-Threshold $I_D$ vs $V_{DS}$

$$I_D = I_0e^{\frac{qV_{GS}}{nkT}} \left( 1 - e^{\frac{qV_{DS}}{kT}} \right) 1 + \lambda \cdot V_{DS}$$
Summary of MOSFET Operating Regions

- **Strong Inversion** $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- **Weak Inversion (Sub-Threshold)** $V_{GS} \leq V_T$
  - Exponential in $V_{GS}$ with linear $V_{DS}$ dependence
Parasitic Resistances

\[ G \]

\[ V_{GS} \]

\[ S \]

Polysilicon gate

Drain contact

Drain
Latch-up

(a) Origin of latchup

(b) Equivalent circuit
Future Perspectives

25 nm FINFET MOS transistor
Problems HW3

1. Rabaey Chap. 3 on-line problems: 2, 3 (do not do the spice simulation), 6, 9 (L=0.5um)

2. Consider an inverter built with 1/0.5 (nmos W/L) and 2/0.5 (pmos) transistors. Draw a sue schematic for the inverter driving a 10fF load capacitor (other terminal is grounded). Using your model for the AMI FET transistors, determine the peak current flowing into the FET after both an abrupt rising and falling edge on the inverter input, given a supply voltage of 3.3 Volts and using the Mosis extracted parameters from the MOSIS or the class website. Simulate these transitions using spice from the Sue schematic.

3. Complete the Max layout of the full adder cells and build a schematic in sue for each cell and for an 8-bit ripple carry adder. Be sure to use the same transistor sizes in the schematic as you had in your layout. Simulate the adder for the following transition: a=0->1, b=255 Plot the sum and carry outputs and estimate the total carry chain delay and delay per stage.