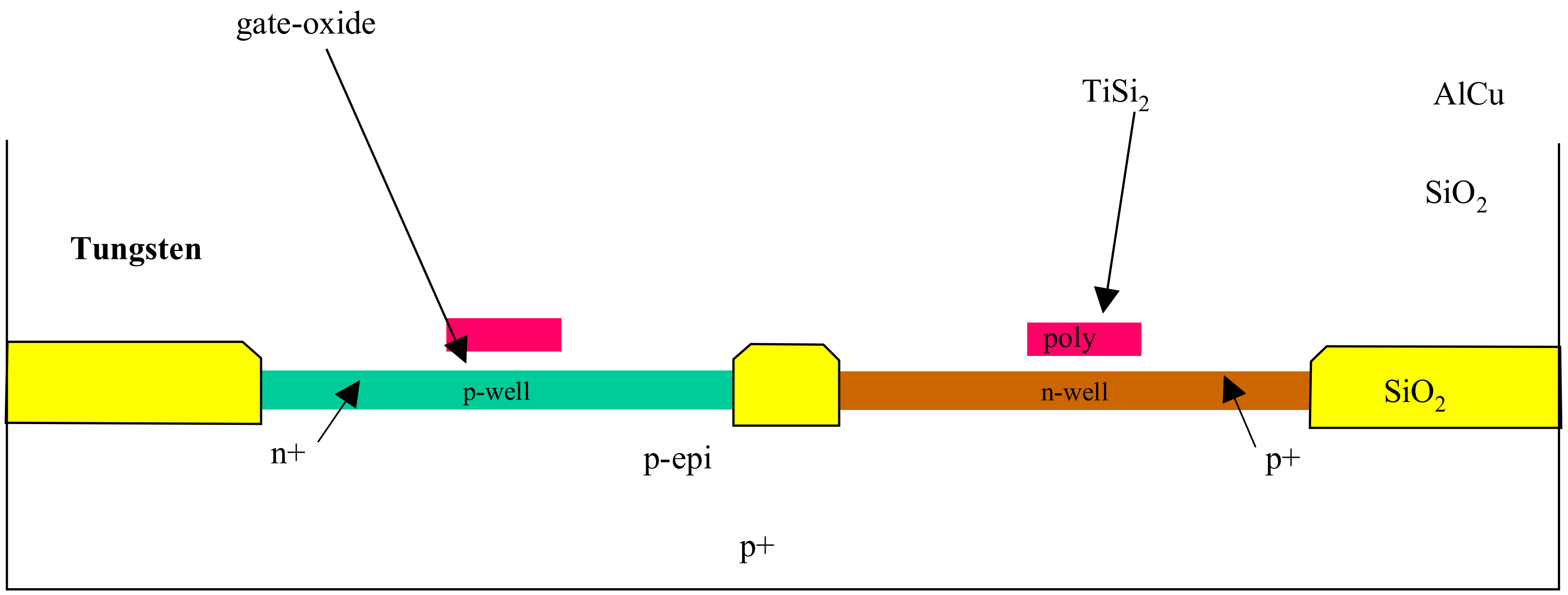
ECE 224a
Process and Design Rules

- ☐ Process Overview
- ☐ Device Fabrication Limits
- ☐ Derived Layers
- ☐ Self Alignment/Dual Damascene/CMP
- ☐ Design Rules
  - Resolution/Step Coverage/Process
  - Electrical/Reliability/Mechanical Stress

A Modern CMOS Process



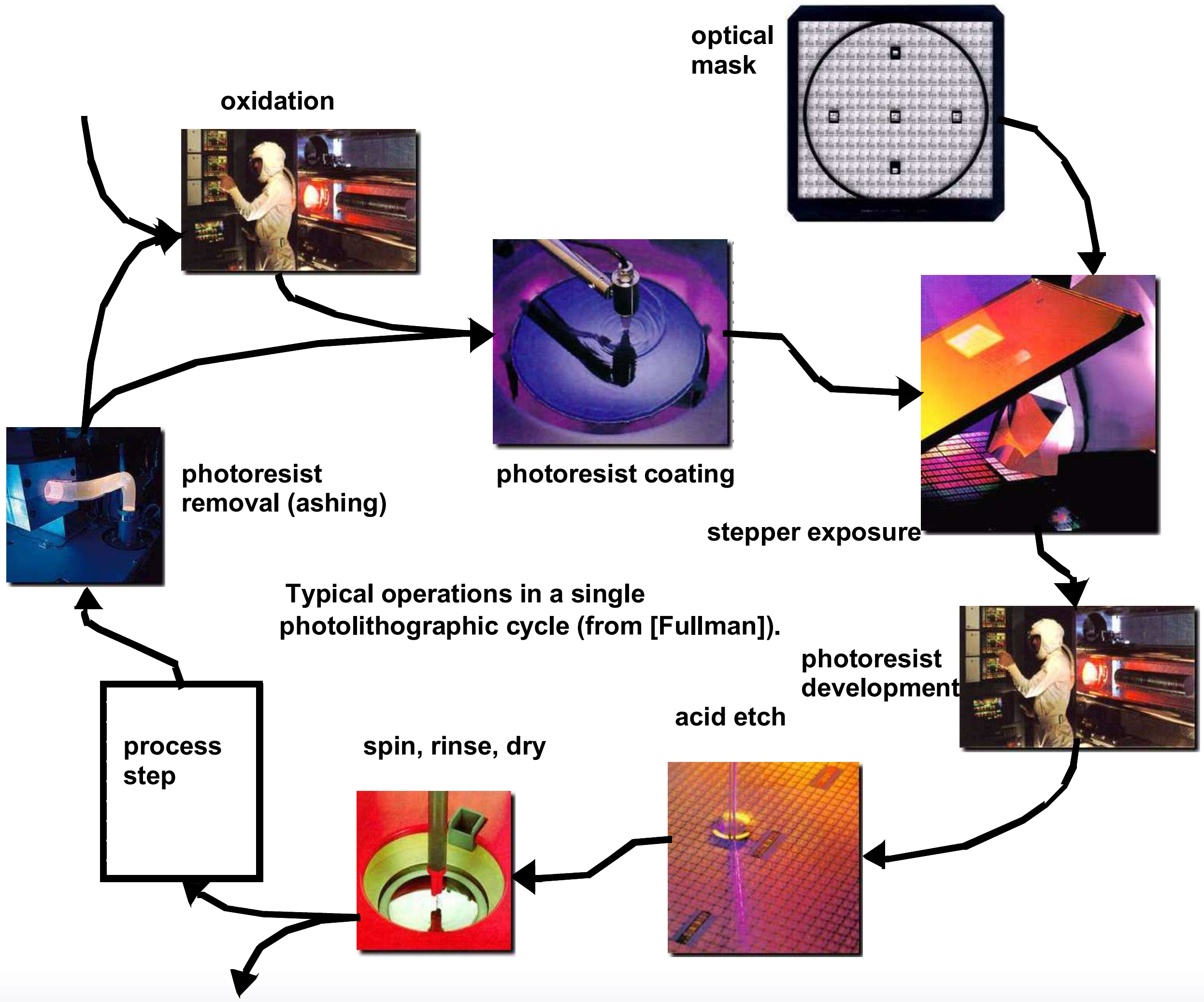
Dual-Well Trench-Isolated CMOS Process

The Manufacturing Process

- ❑ Photo-Lithography
  - Mask to Resist
  - Resist to Pattern Layer
  - Process (Implant/Etch/Oxide/Nitride/…)
  - Cleanup (Clean/Planarization/Anneal)
  - Setup next Layer for Processing

For a great reference source:
http://www.reed-electronics.com/semiconductor

Photo-Lithographic Process



oxidation

optical
mask

photoresist coating

stepper exposure

photoresist
development

acid etch

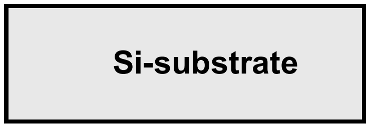
spin, rinse, dry

process
step

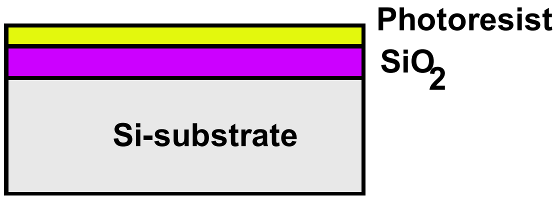
photoresist
removal (ashing)

Typical operations in a single photolithographic cycle (from [Fullman]).

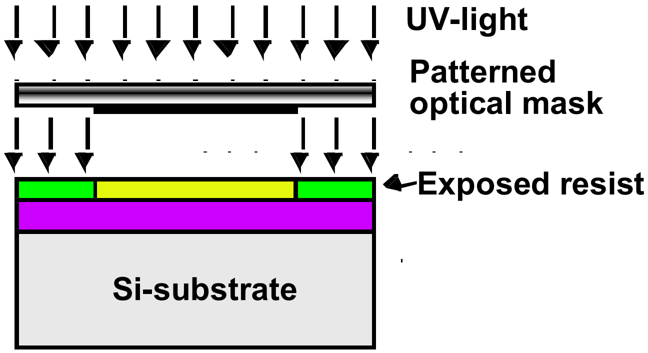
Patterning of SiO2



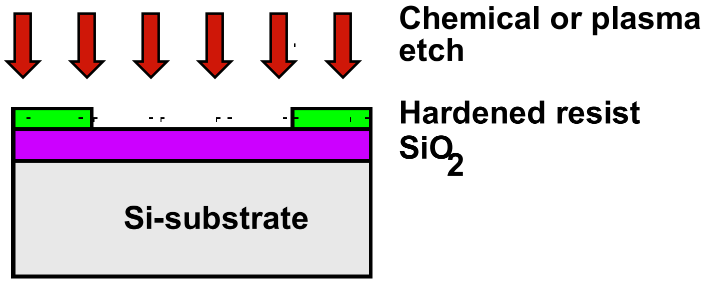
(a) Silicon base material



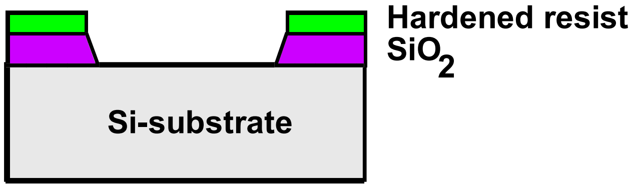
(b) After oxidation and deposition of negative photoresist



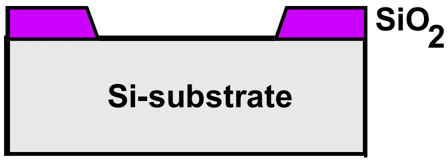
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

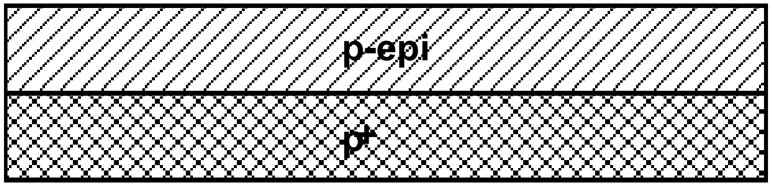


(e) After etching

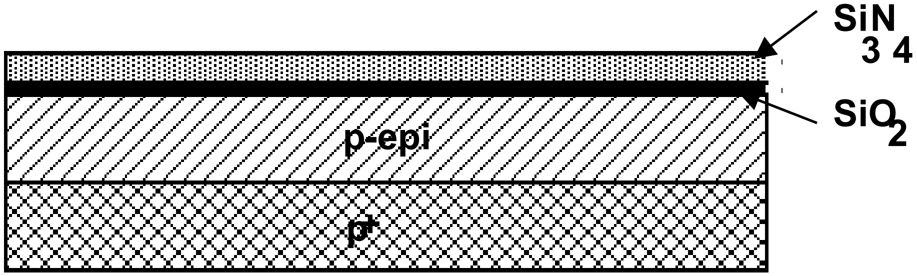


(f) Final result after removal of resist

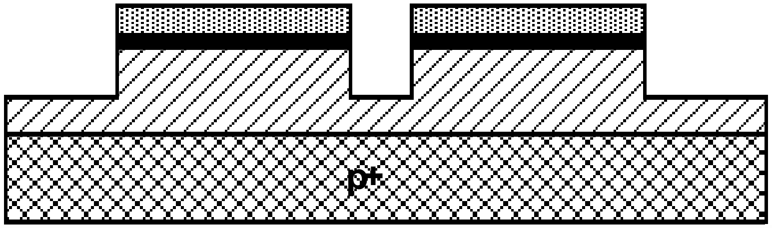
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

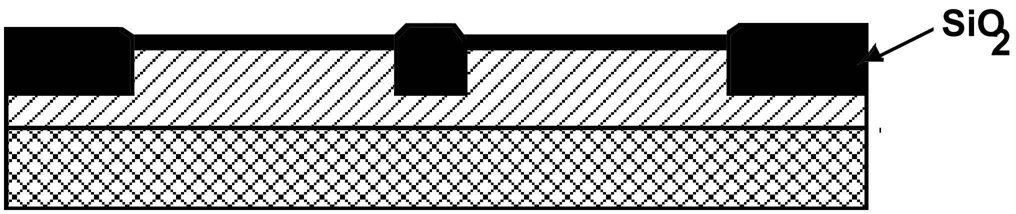


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

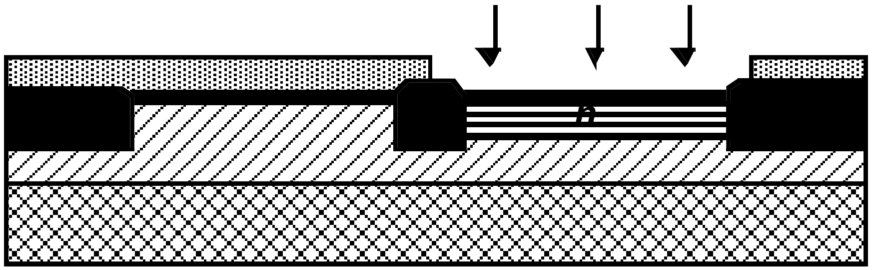


(c) After plasma etch of insulating trenches using the inverse of the active area mask

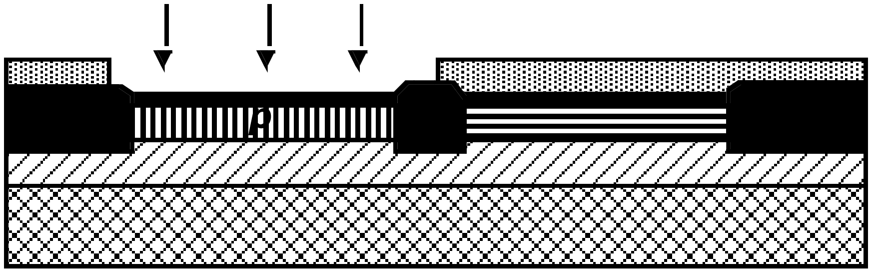
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

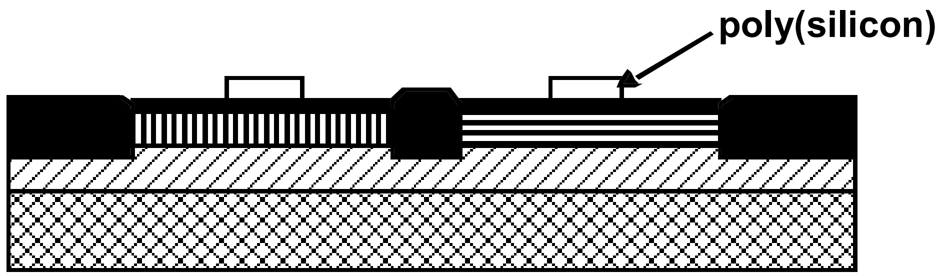


(e) After n-well and V_{Tp} adjust implants

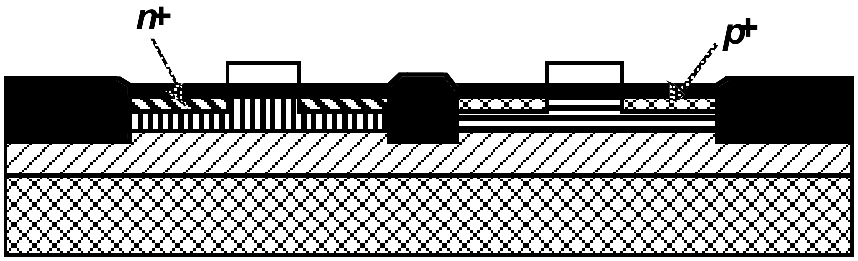


(f) After p-well and V_{Tn} adjust implants

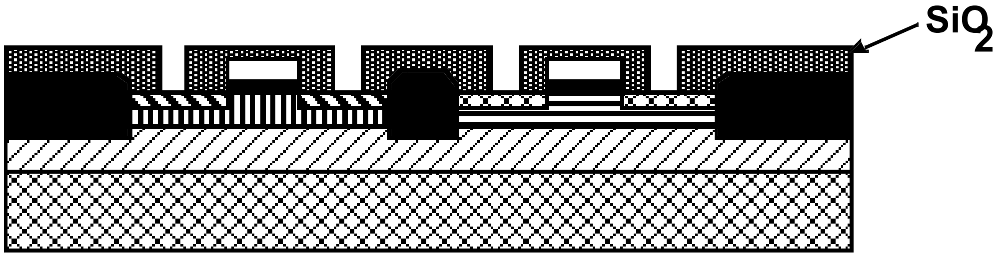
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

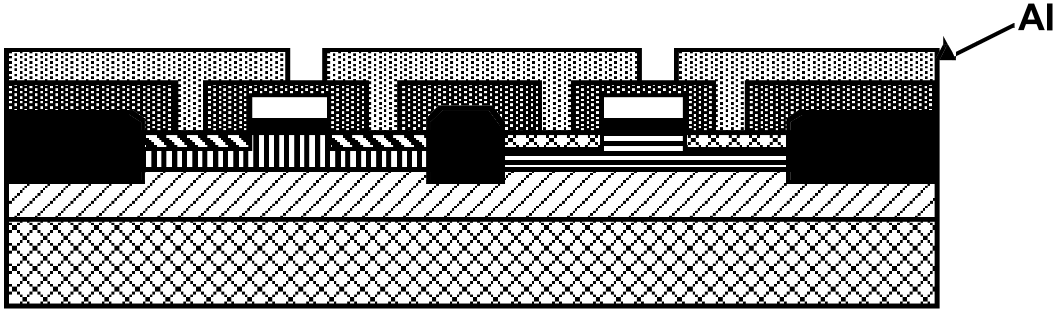


(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.

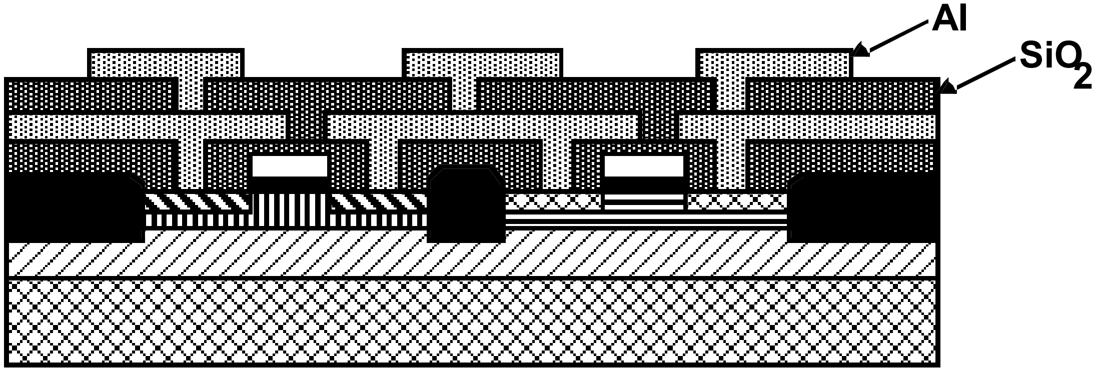


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through



(j) After deposition and patterning of first Al layer.

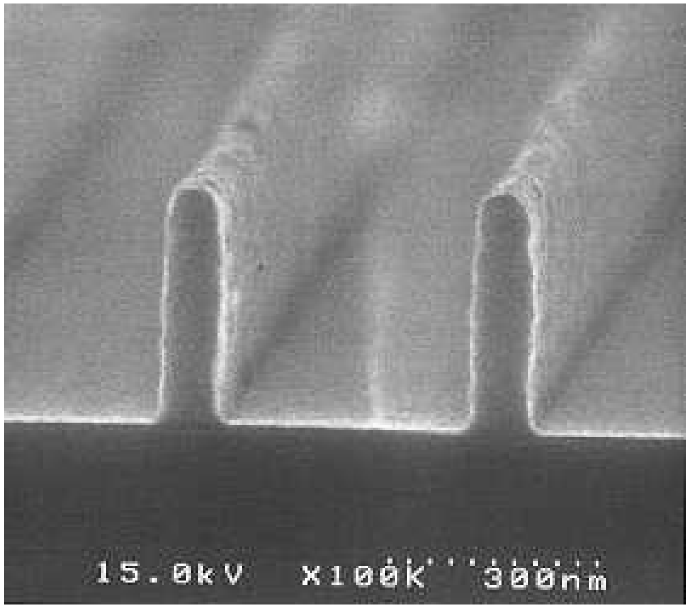


(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

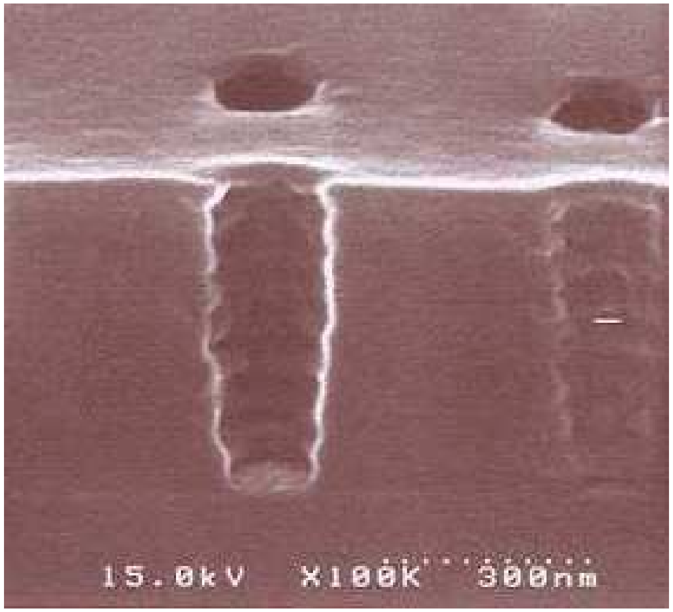
Advanced Process Modules

Generation	0.25um	0.18um	0.15um	0.13um	0.1um
Isolation	STI				
Substrate	Bulk/Epi			SOI option	
Well	Retrograde --> Advanced SSR				
Gate Dielectric	Multiple Gate Dielectric (Core/IO & Mixed-Signal)				
Gate	Dual Poly (n+/p+) Salicide				
Gate Litho	DUV 248nm		PSM	193nm PSM	
Junction Engineering	Advanced Junction/Pocket Engineering				
Silicide	TiSix	CoSix			NiSix
BEOL Metal	Al	Al and Cu		Cu	
BEOL Dielectric		Low-k (k=3.7)		(K<3.0)	(K<2.5)

Lithography for 0.1um Node

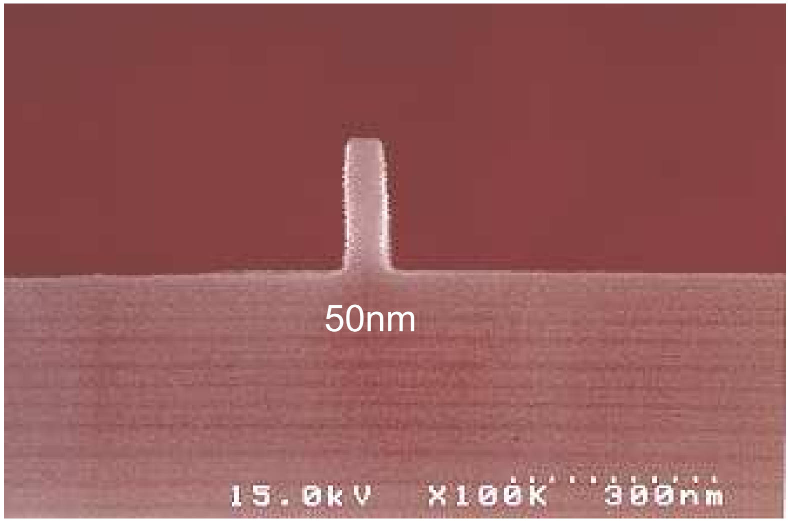


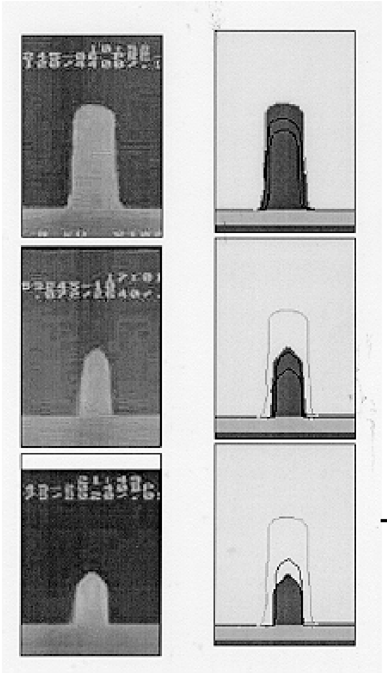
80 nm Lines



120 nm Contact Holes

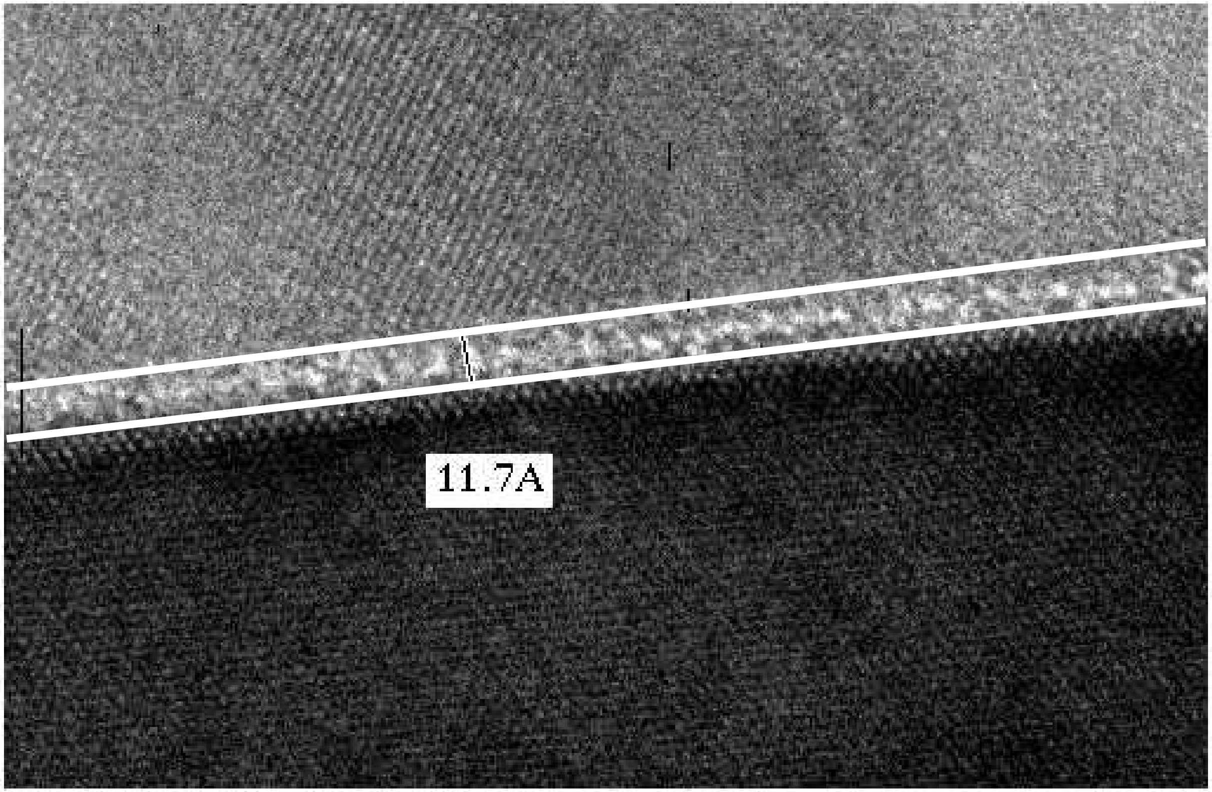
Poly Gate Etch ≤ 100nm





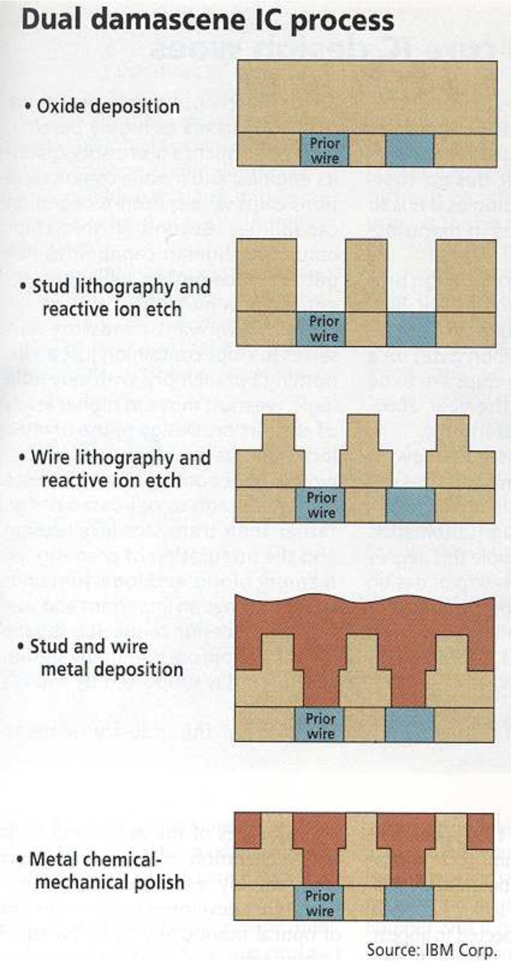
Resist trimming is predictable by computer simulation as well as experiment.

12A Gate Oxide



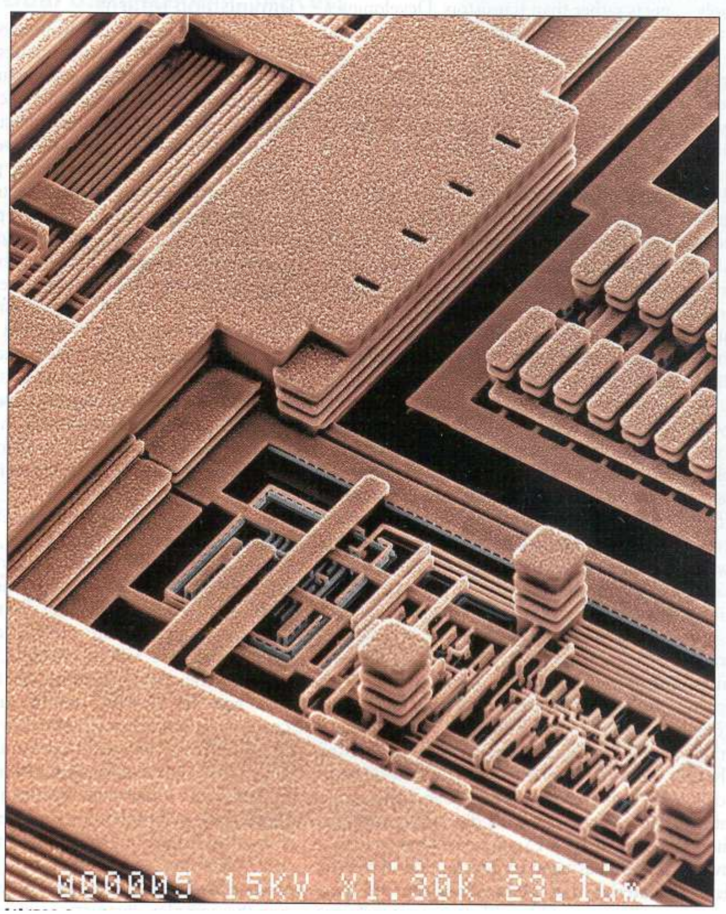
000332_DC&RB_K12_2

Advanced Metallization

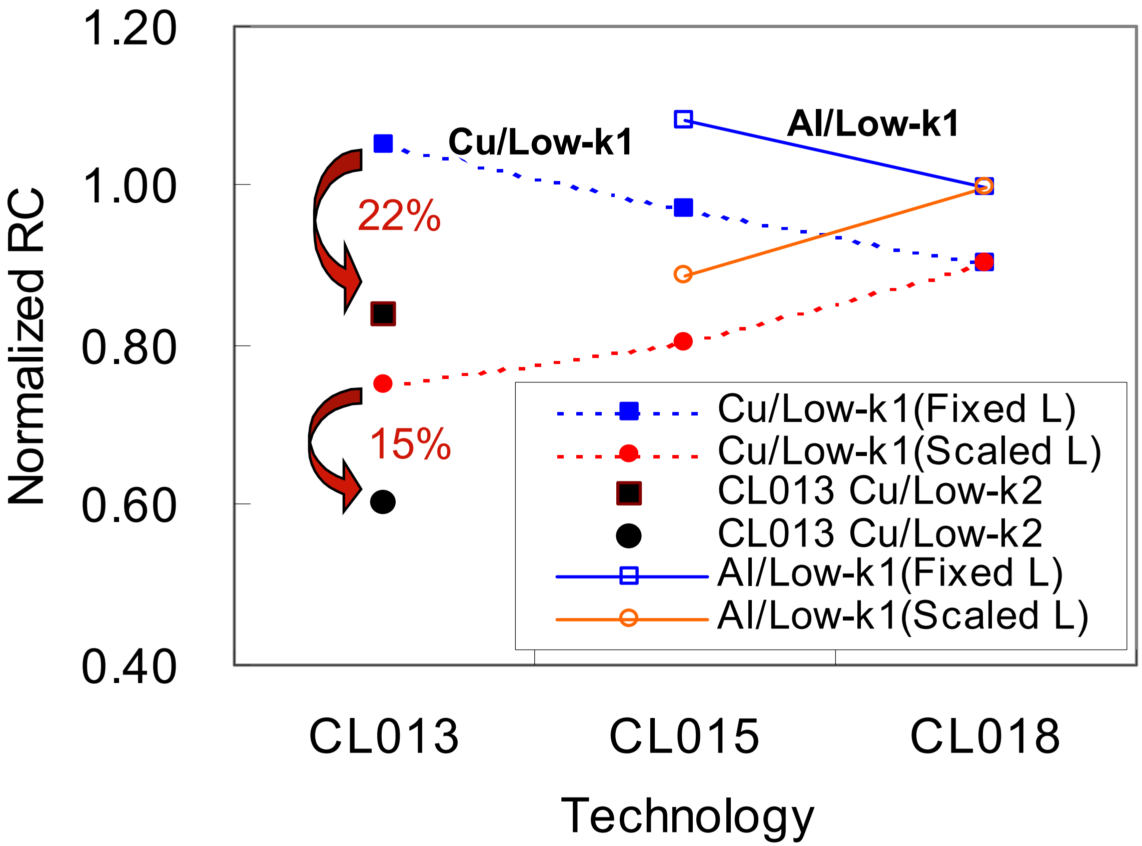


Dual damascene IC process

Source: IBM Corp.



Interconnect RC Trend



- RC delay is evaluated at minimum M2 pitch

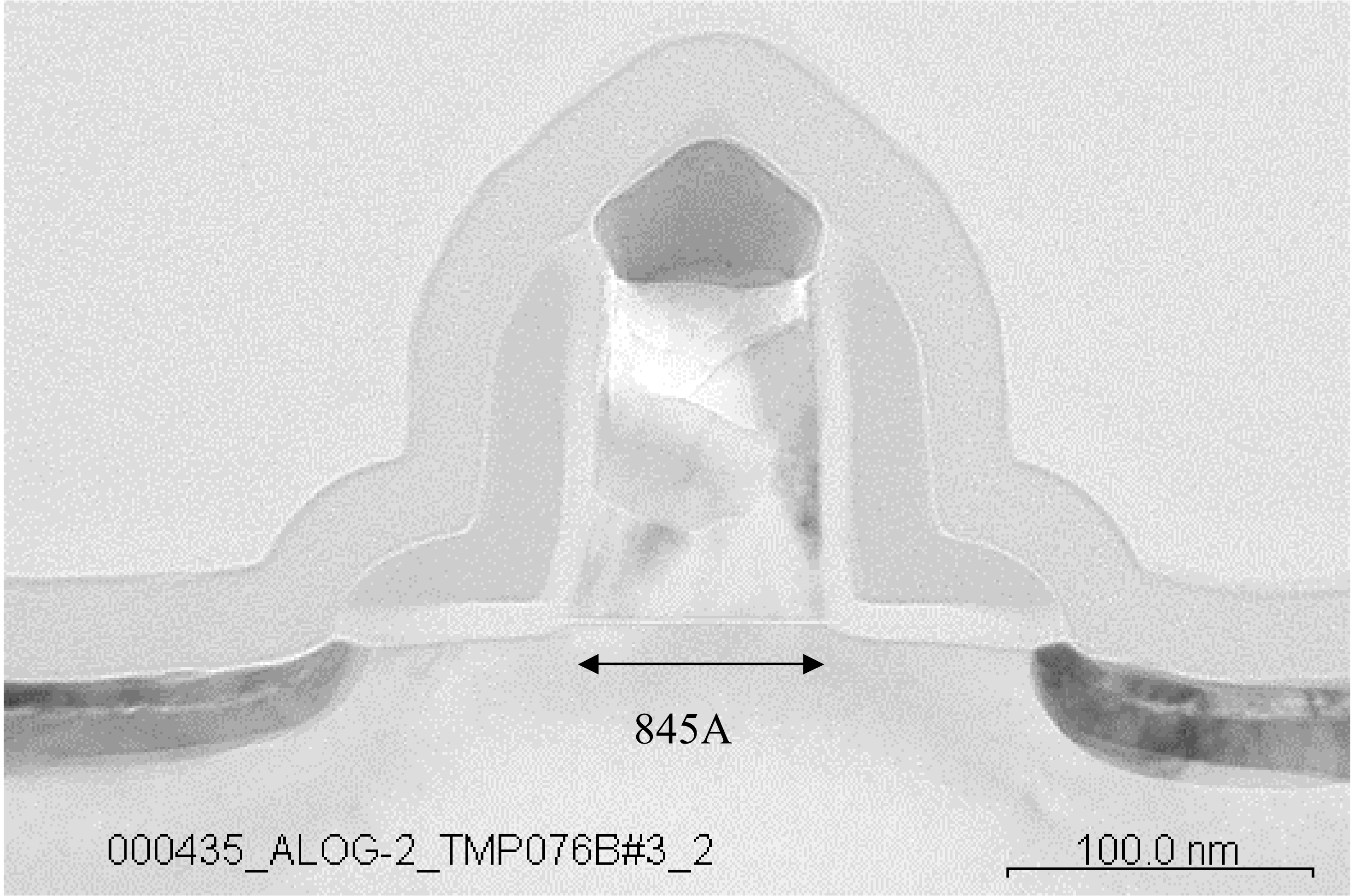
Design Rules

- ❑ What can be fabricated?
  - Resolution Limits
    - Light Source (357nm, 254nm, 193nm, ?)
    - Contact/Phase Masking
    - Surface State (Reflection/Scattering)
  - Material Limits
    - Step Coverage
    - Porosity/Defect Propagation
    - Mechanical/Thermal Stress

Design Rules II

- Electrical Limits
  - Electrical Fields (MV/cm)!
  - Parasitic Conductivity/Devices (Latchup/ESD)
  - Joule Heating (Electro-Migration)
- Defect Probability
  - Contact/Via Replication
  - Grid-Based Power/Ground Networks
- Advance Lithography
  - Rule Explosion/Failure of Locality
  - CMP Area Rules/Antenna Rules

85nm Poly Gate Profile



CL013 Core Device

Technology	CL013LV (14 ps/gate* (		CL013G (20 ps/gate* (	
Vcc	1.0V NMOS	1.0V PMOS	1.2V NMOS	1.2V PMOS
Lg (um)	0.08	0.085	0.12	0.12
Idsat(uA/um)	610	260	535	225
Vt(V)	0.3	0.3	0.34	0.34
Ioff(nA/um)**	10	10	1	1
BV(V)	>2	>2	>2.4	>2.4

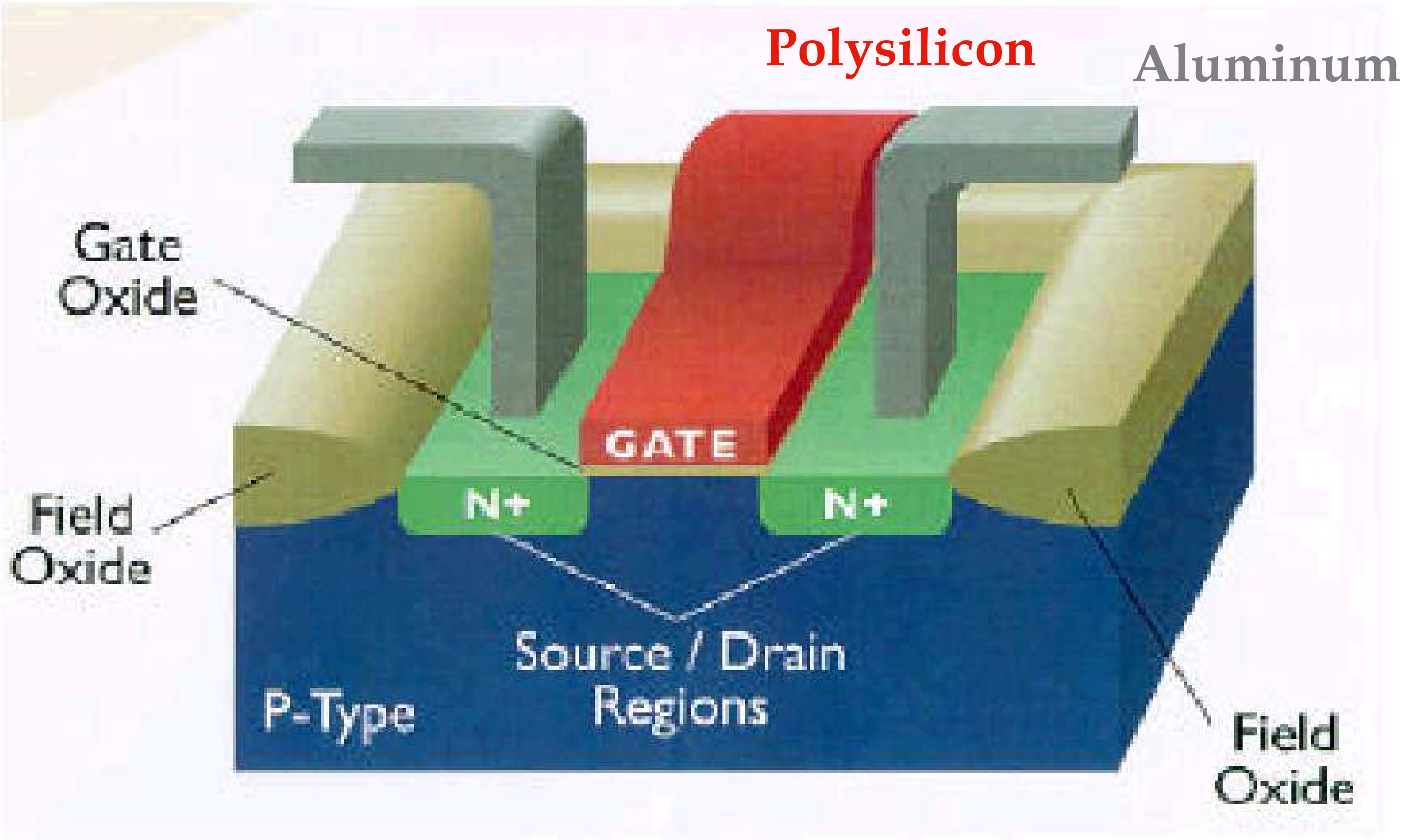
* Fanout = 1 ring oscillator
** room temp. & worst case.

0.13/0.18 Comparison

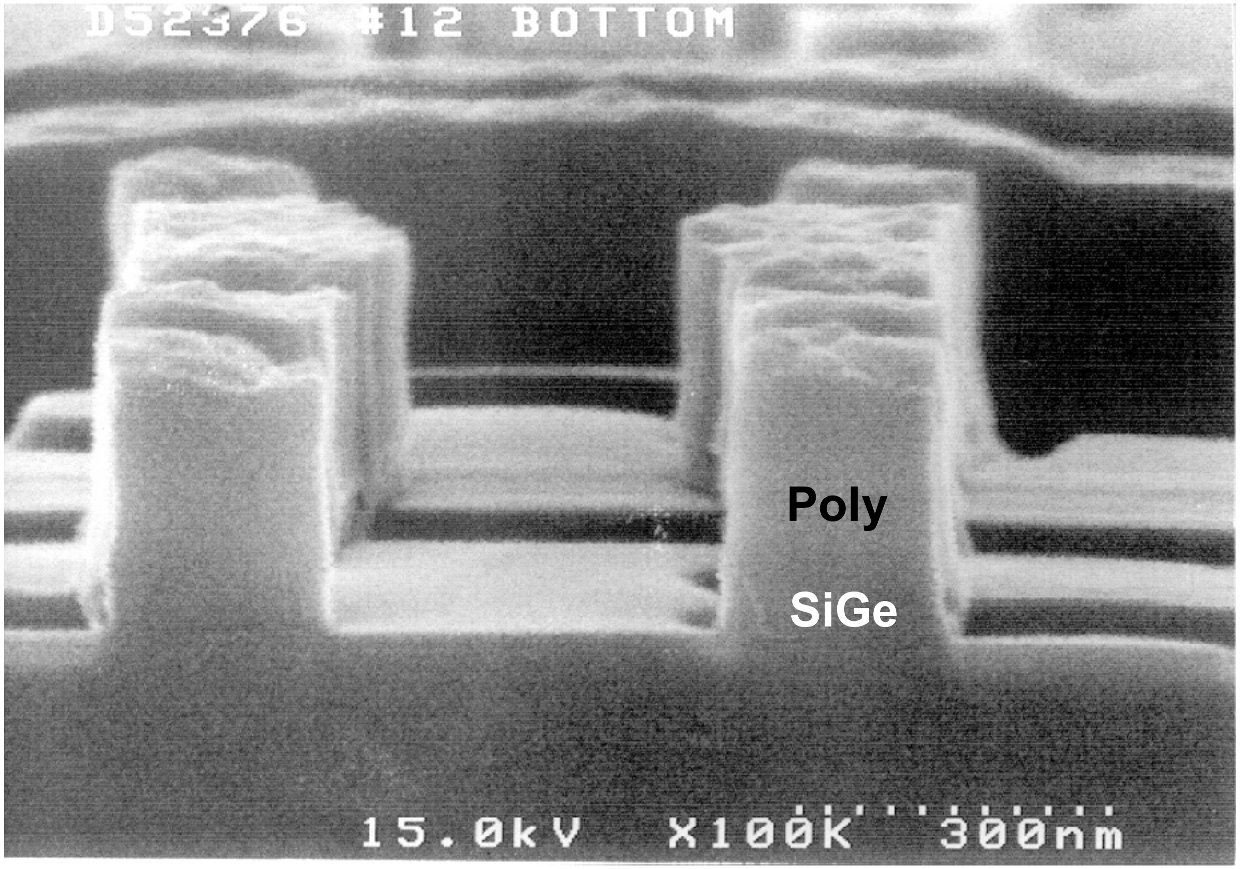
Rule/Technology (unit: um)	CL018 1P6M	CL013 1P8M	Shrink Ratio(%) CL018 => CL013
N+/P+ spacing	0.86	0.62	72.0
OD (W/S)	0.22/0.28	0.15/0.21	72.0
Poly (W/S)	0.18/0.25	0.13/0.18	72.1
CO (W/S)	0.22/0.25	0.16/0.18	72.3
M1 (W/S)	0.23/0.23	0.16/0.18	73.9
Via1-Via (n-2) (W/S)	0.26/0.26	0.19/0.22	78.8
M2 ~ M(n-1) (W/S)	0.28/0.28	0.20/0.21	73.2
Via(n-1) (W/S)	0.36/0.35	0.36/0.35	100.0
Mn (W/S)	0.44/0.46	0.44/0.46	100.0
6T SRAM Cell (um^2)	4.65	2.43	52.3

* Please refer to shrinkage guideline for non-shrinkable details

3D Perspective



Poly-SiGe Gate



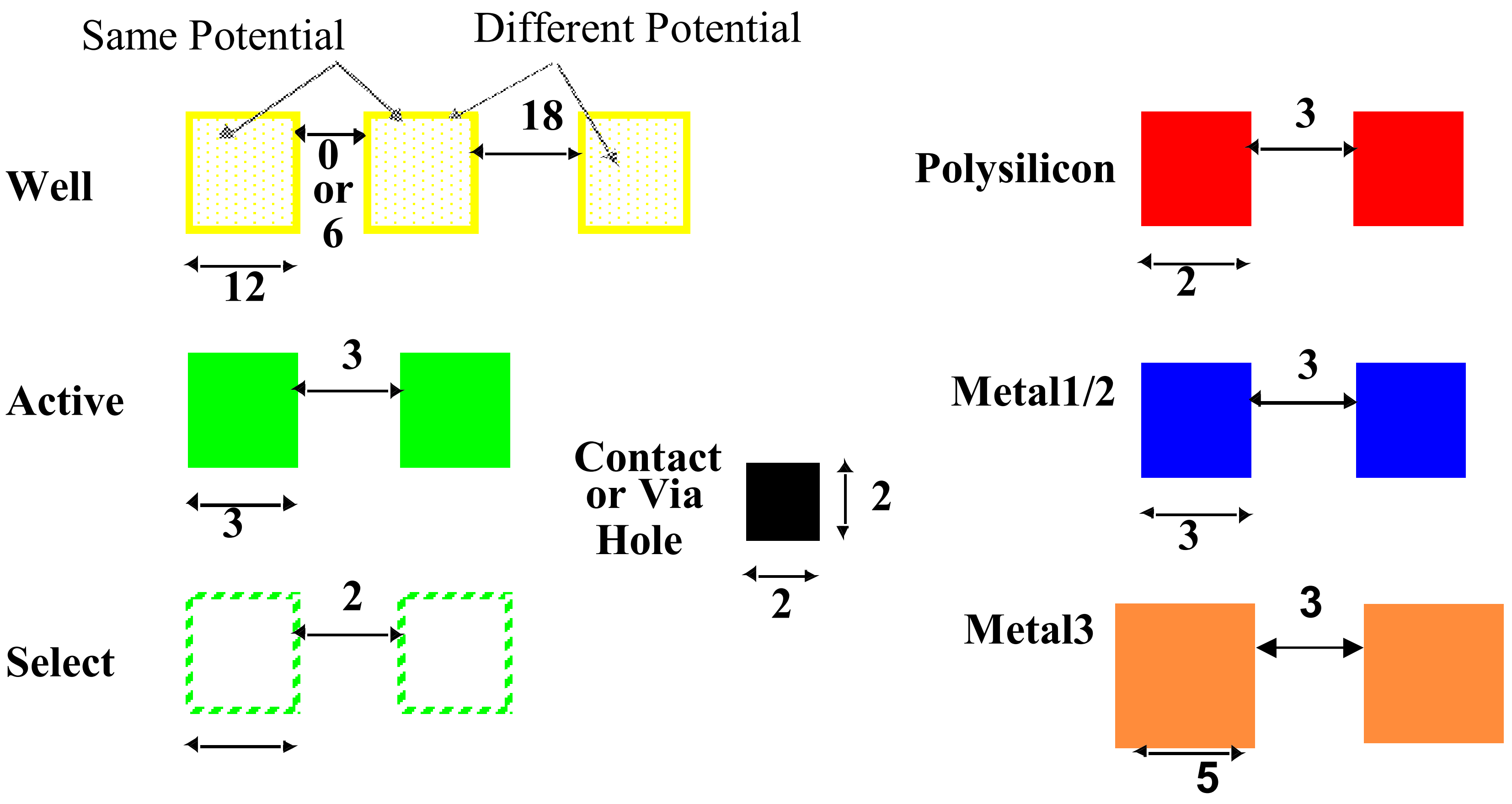
Design Rules III

- ❑ Interface twixt designer and process engineer
- ❑ Unit dimension: Minimum Feature Size
  - scalable design rules: lambda
  - absolute dimensions: (Vendor rules)
- ❑ Process Design Layers
  - Derived Layers

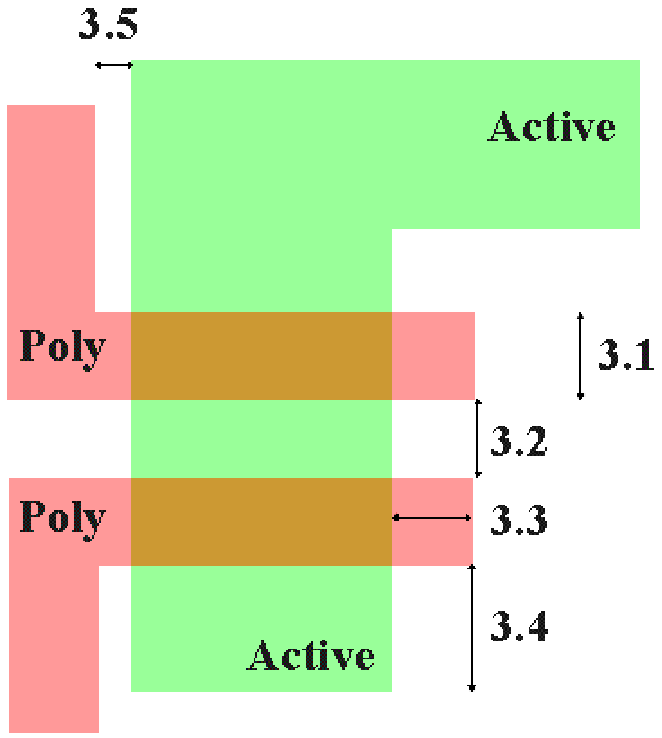
CMOS Process Design Layers

Layer	Color	Representation
Well (p,n)	Yellow	▭
Active Area (n+,p+)	Green	🟩
Select (p+,n+)	Green	⬚
Polysilicon	Red	🟥
Metal1	Blue	🟦
Metal2	Magenta	🟪
Metal3	Gold	🟧
Contact to poly/diff	Black	⬛
Vias	Black	⬛

Intra-Layer Design Rules



Transistor Layout



3.1 FET length 2 (min)

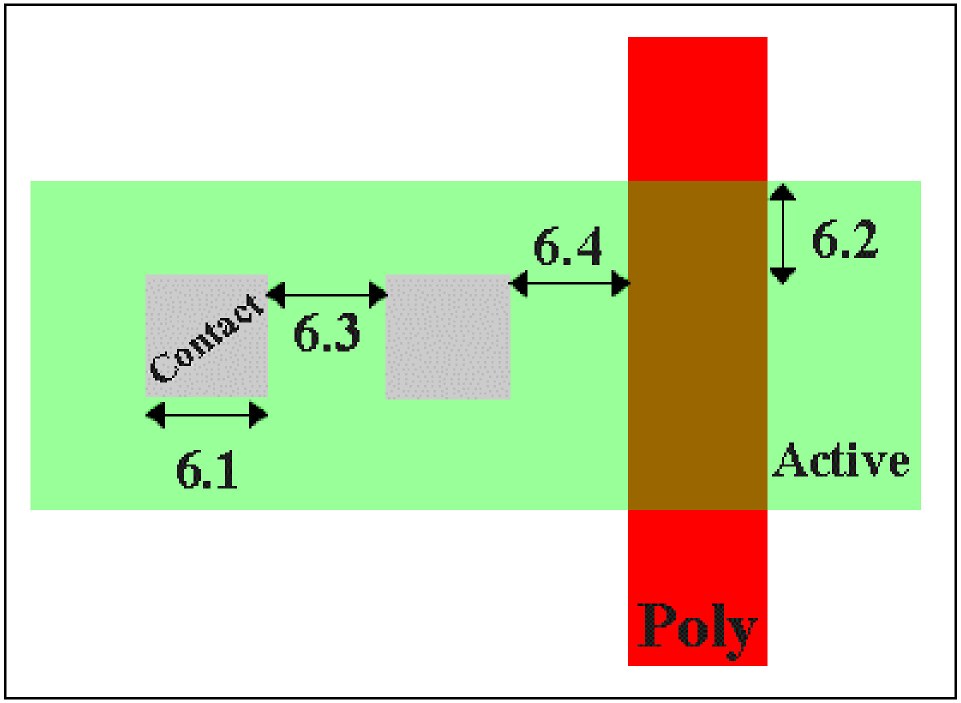
3.2 FET spacing 3

3.3 Poly Overlap 2

3.4 Active Overlap 3

3.5 Space 1

Active Contact I



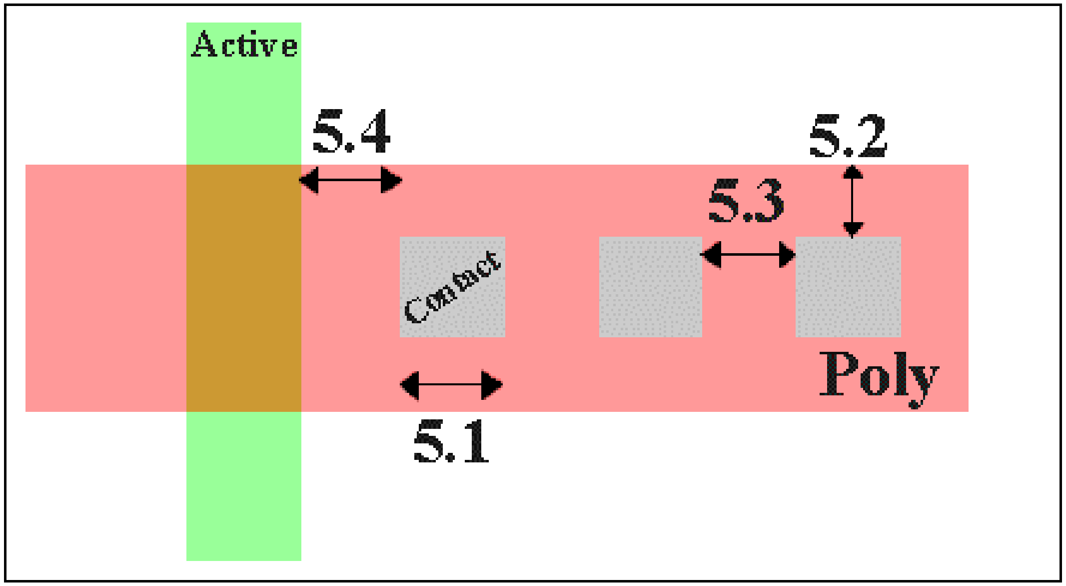
6.1 Size 2x2

6.2 Enclosure 1.5

6.3 Spacing 3

6.4 Space to FET 2

Poly Contact I



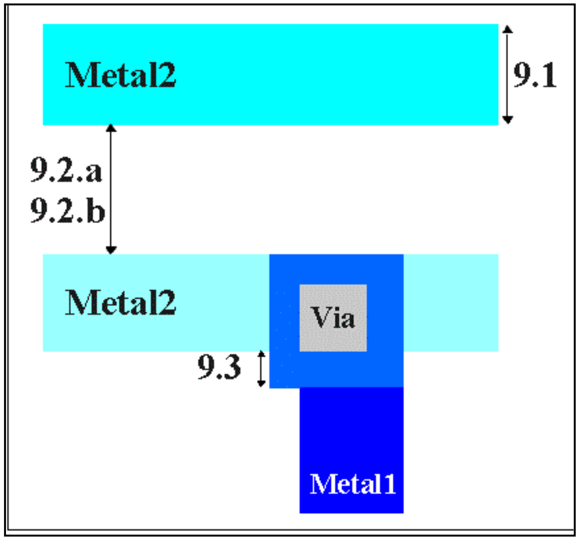
5.1 Size 2x2

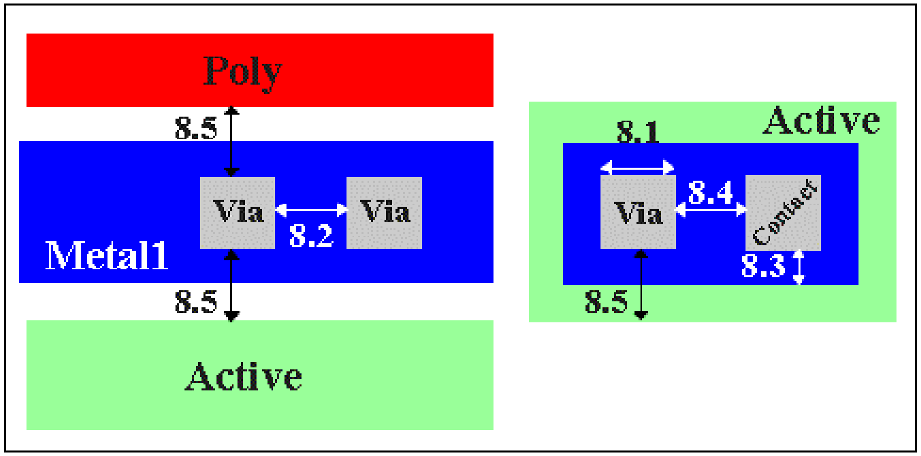
5.2 Enclosure 1.5

5.3 Spacing 3

5.4 Space to FET 2

Via (m1 to m2)

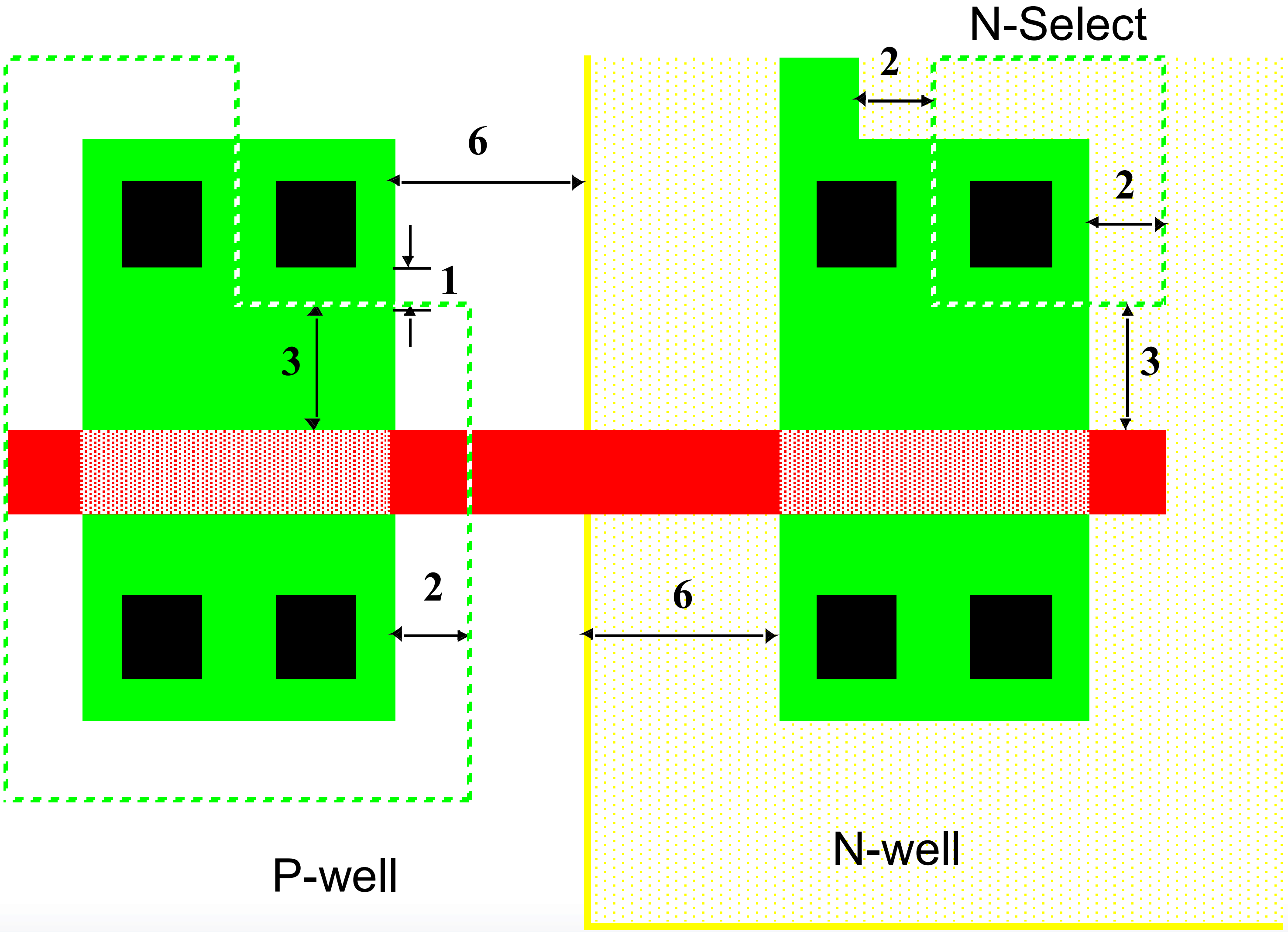




9.1 Min Width 3
9.2.a Spacing 3
9.2.b Spacing 6 (width>10)
9.3 Enclosure 1

8.1 Size 2x2
8.2 Spacing 3
8.3 Enclosure 1
8.4 Space to Contact 2
8.5 Space to Poly/Act 2

Select Layer



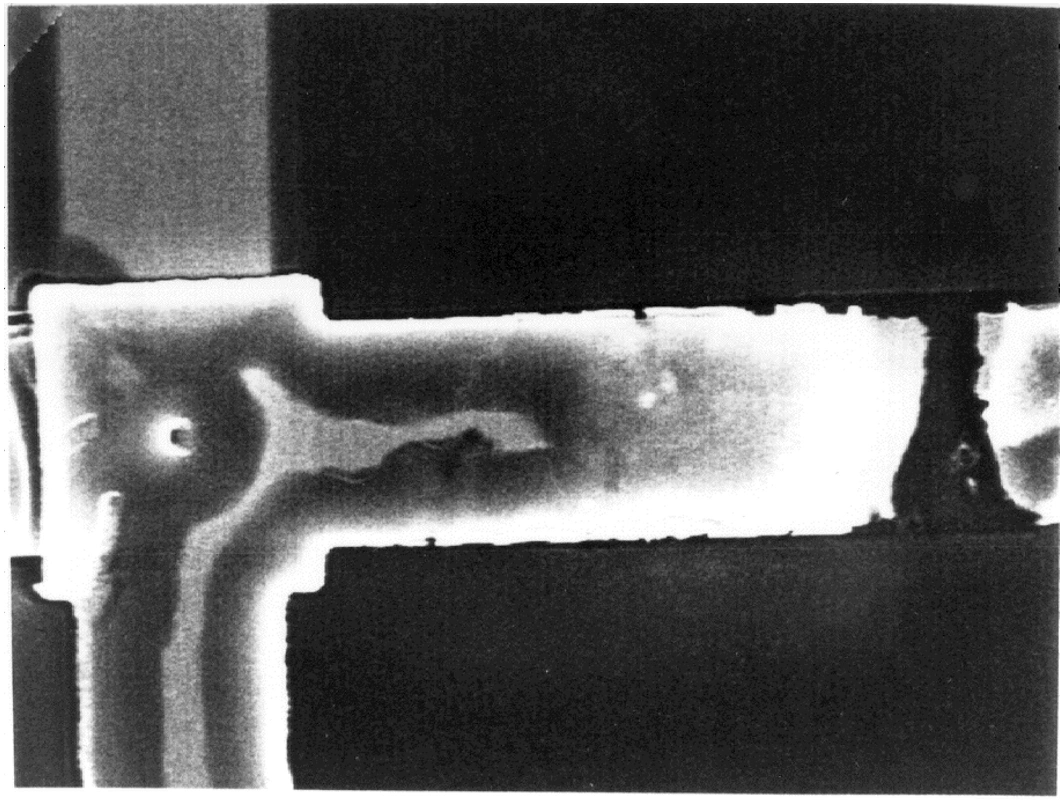
CMP Density Rules

- ❑ Chemical-Mechanical Polishing
  - Requires uniform density of metal/poly
- ❑ SCMOS Rules:
  - Poly 30% density across each 1mm^2 area
  - M1, M2 15% density
  - M3 (top metal) is not restricted since no further polishing…

Layout Guidelines I

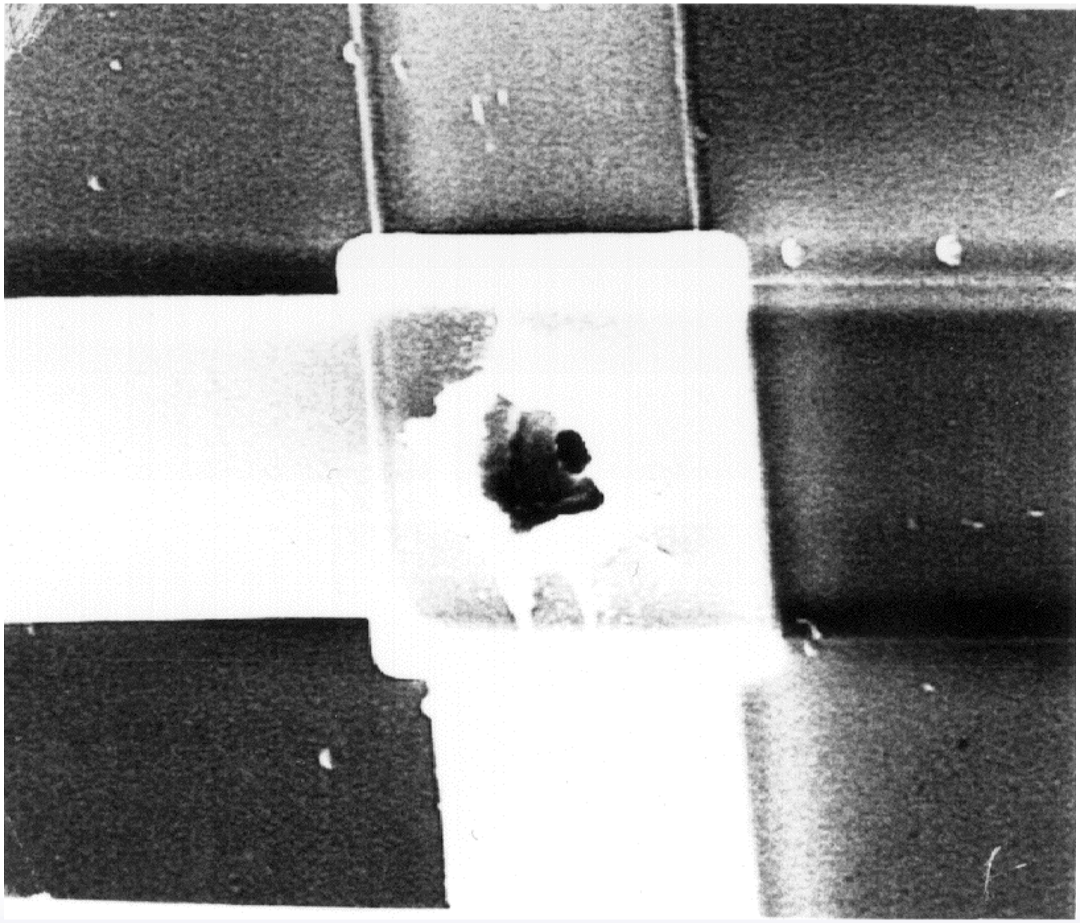
- Group Transistors into Cells
  - Plan inter-cell wires first (Sticks)
  - Oversize Power Grids (Cell Default >6)
  - Frequent Substrate Contacts/Well Plugs
    - Every Well (even one will kill design!)
    - Max distance to plug/contact 5-8 microns
- Set a large user grid e.g. 1-2 lambda
  - Don’t optimize until you know the constraints
  - Plan for Change and Optimization

Electromigration (1)



Limits dc-current to 1 mA/μm

Electromigration (2)

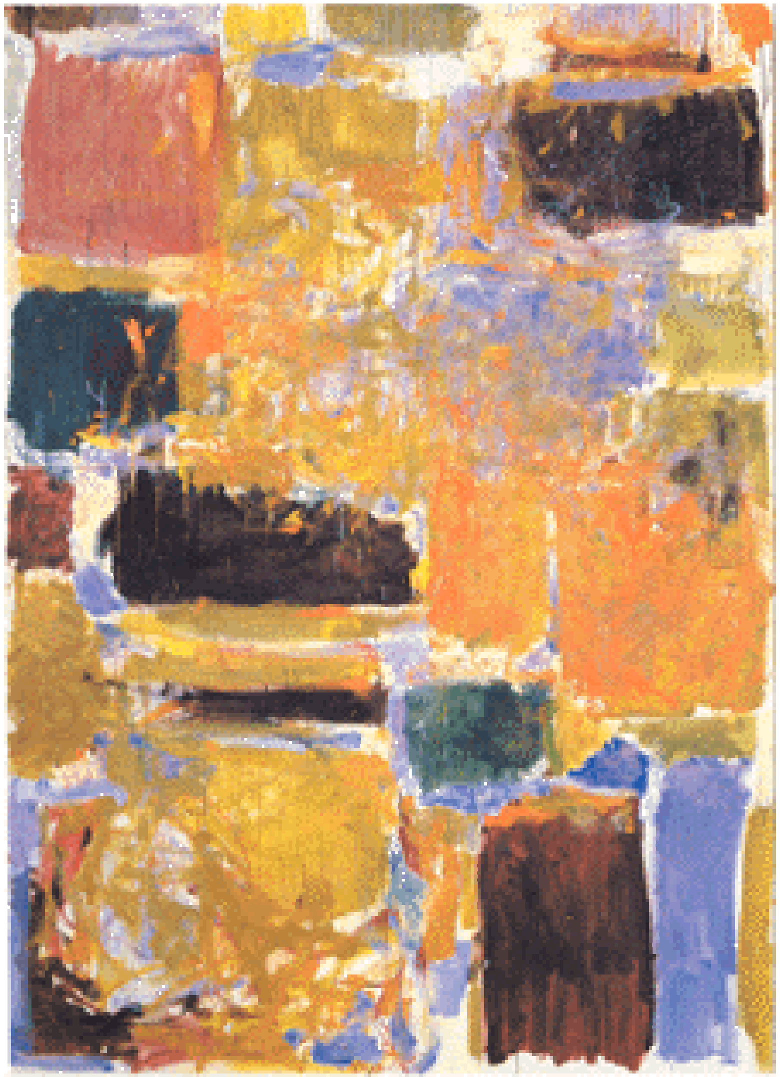


Metal Migration

- ❑ Al (2.9μΩcm M.P. 660 C)
  - 1mA/μm^2 at 60C is average current limit for 10 year MTTF
  - Current density decreases rapidly with temperature
- ❑ Cu (1.7μΩcm M.P. 1060 C
  - 10mA/μm^2 at 100C or better (depends on fabrication quality)
  - Density decreases with temperature, but much slower over practical Silicon operation temperatures <120C
- ❑ Find Average current through wire – check cross section
  - Be wary of Via's!! Typical cross-section: 20-40% of

Layout Guidelines II

- Current Limits
    - 1 mA/μm^2 Avg. current limit (50C)
        - Strongly Temp Dependent (Al)
        - Failures typically occur at vias and contacts
        - Vias often Tungsten (higher resistance)
    - Wide Wires need via arrays!
- Transistor Contacts
    - Active is highly resistive
    - Avoid High Density Currents

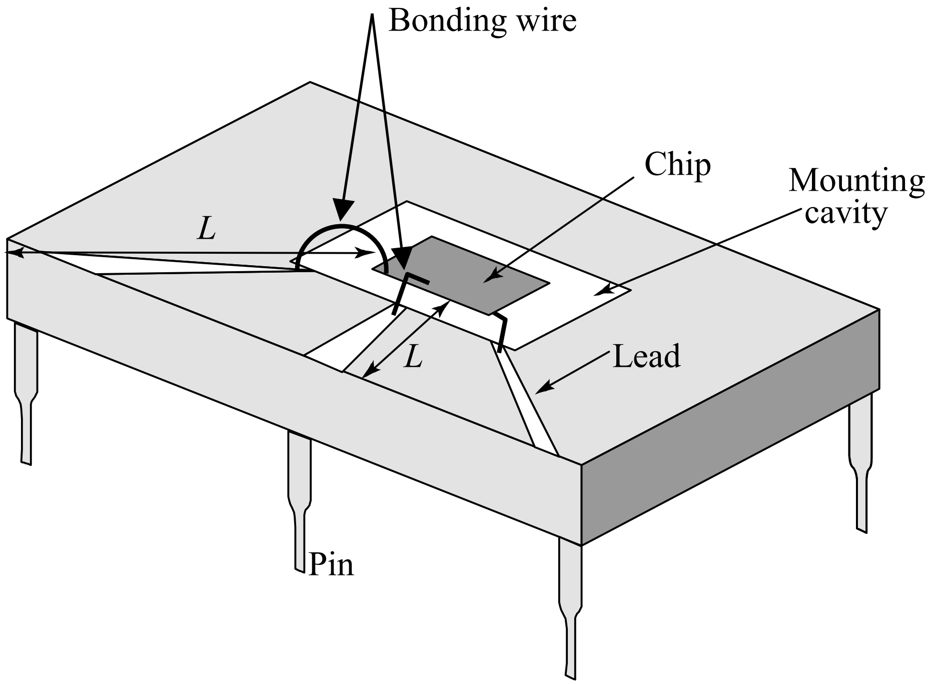


Pads

Pads-- Chip to Board Interface

- Pads drive large Capacitances
  - 5pf minimum to much larger
  - Rise time control
- Board Impeadance and Noise
  - L dI/dt Noise
- Coupling to Power Distribution
- ESD

Chip Packaging



- Bond wires (~25µm) are used to connect the package to the chip

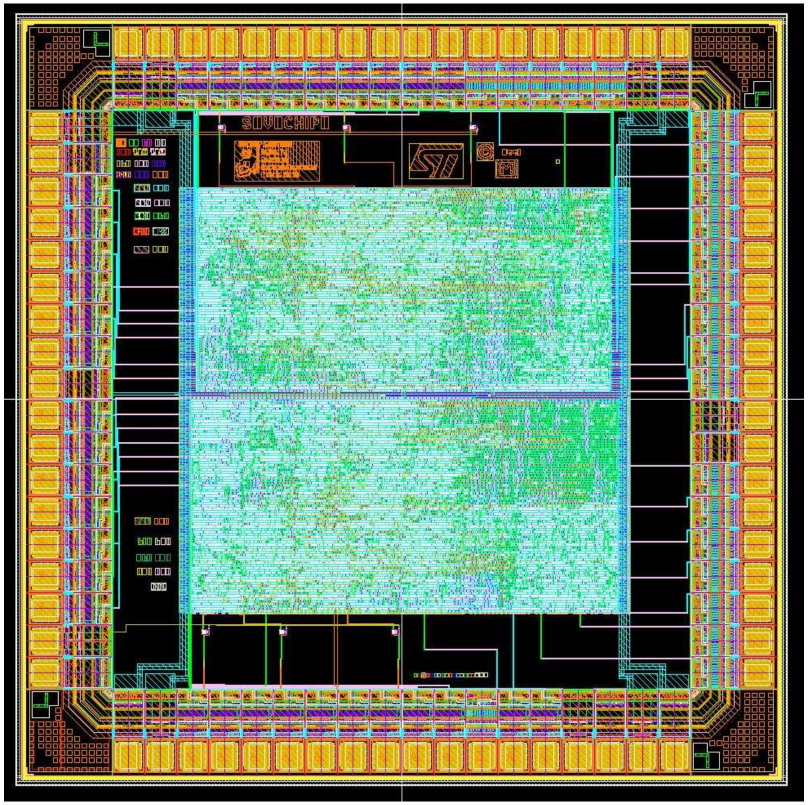
- Pads are arranged in a frame around the chip

- Pads are relatively large (~100µm in 0.25µm technology), with large pitch (100µm)

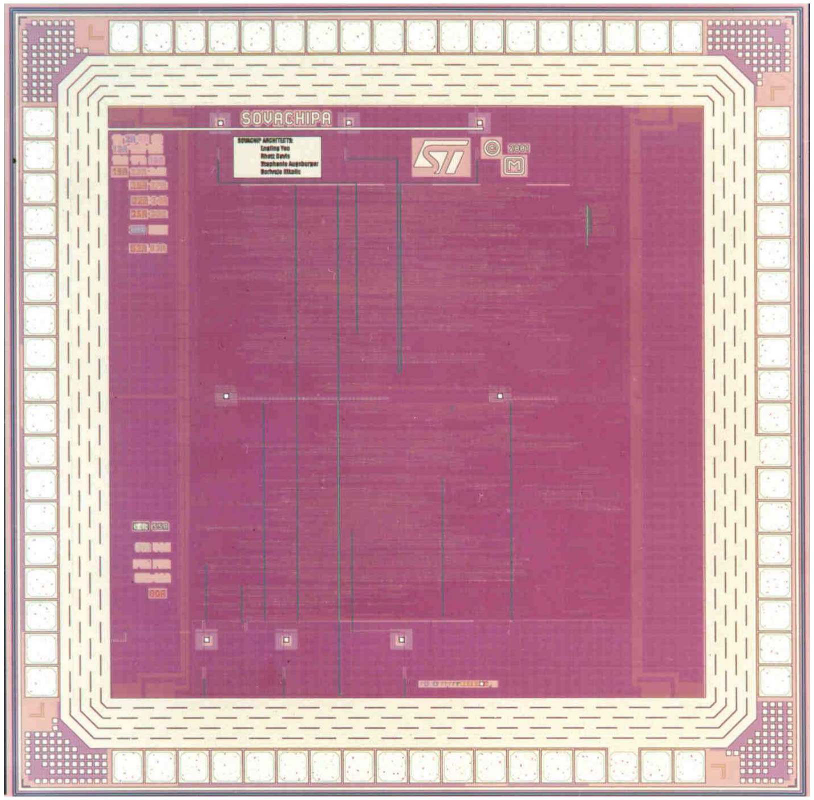
- Many chips areas are 'pad limited'

Pad Frame

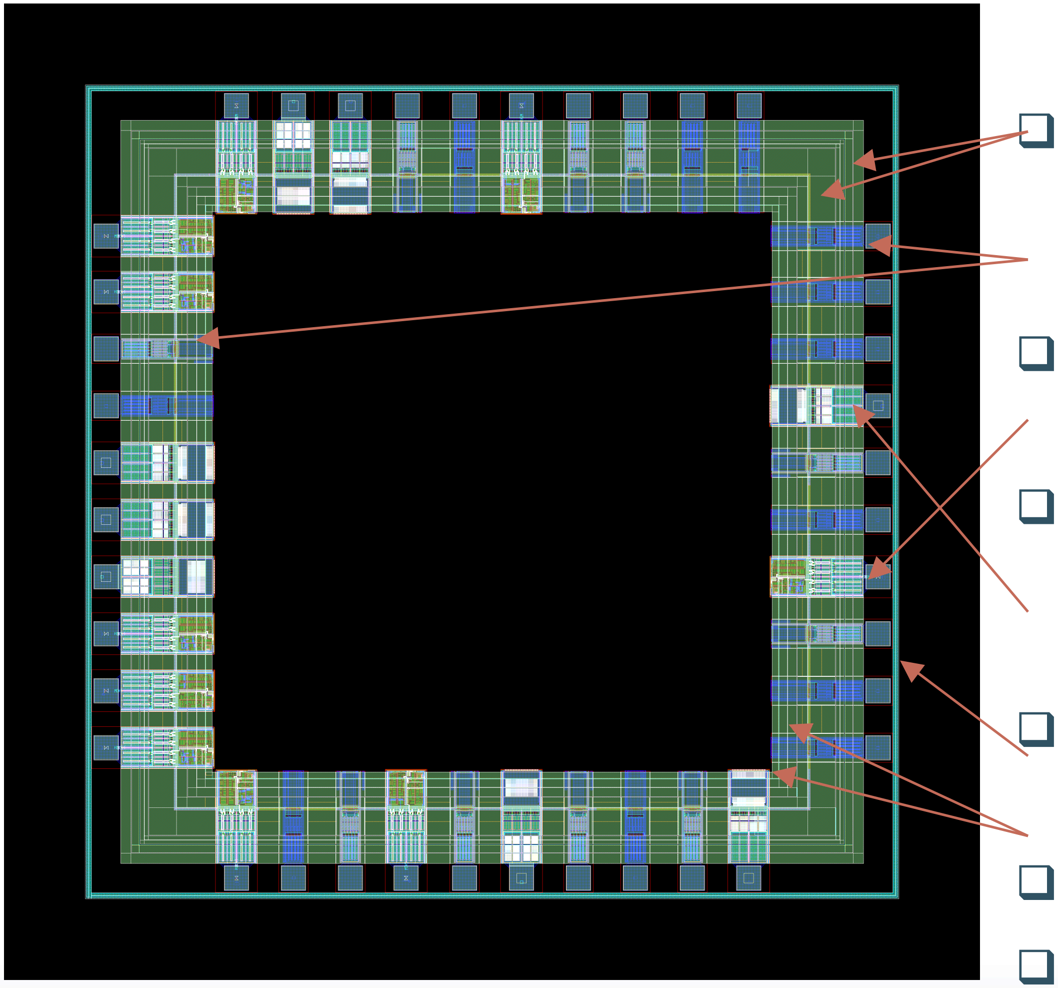
Layout



Die Photo

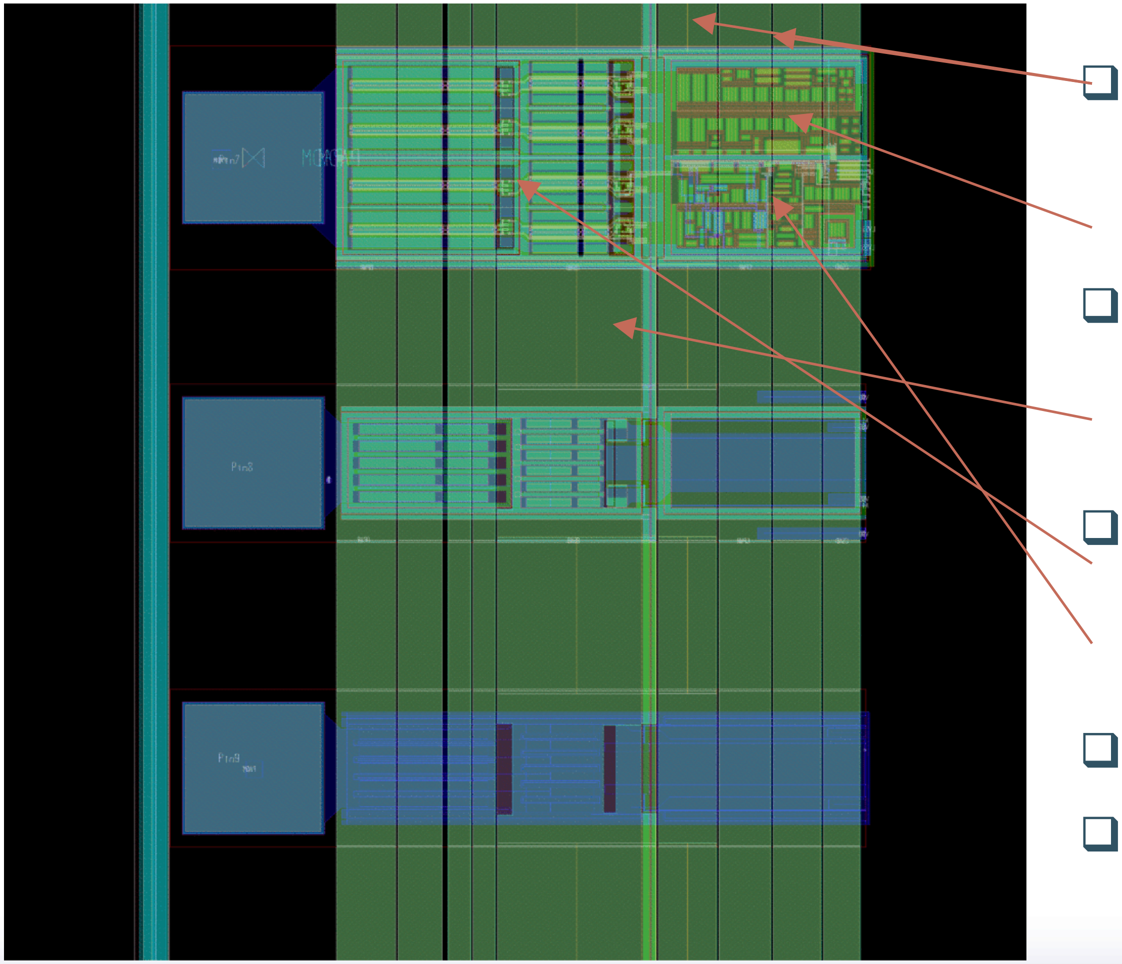


Pad Example



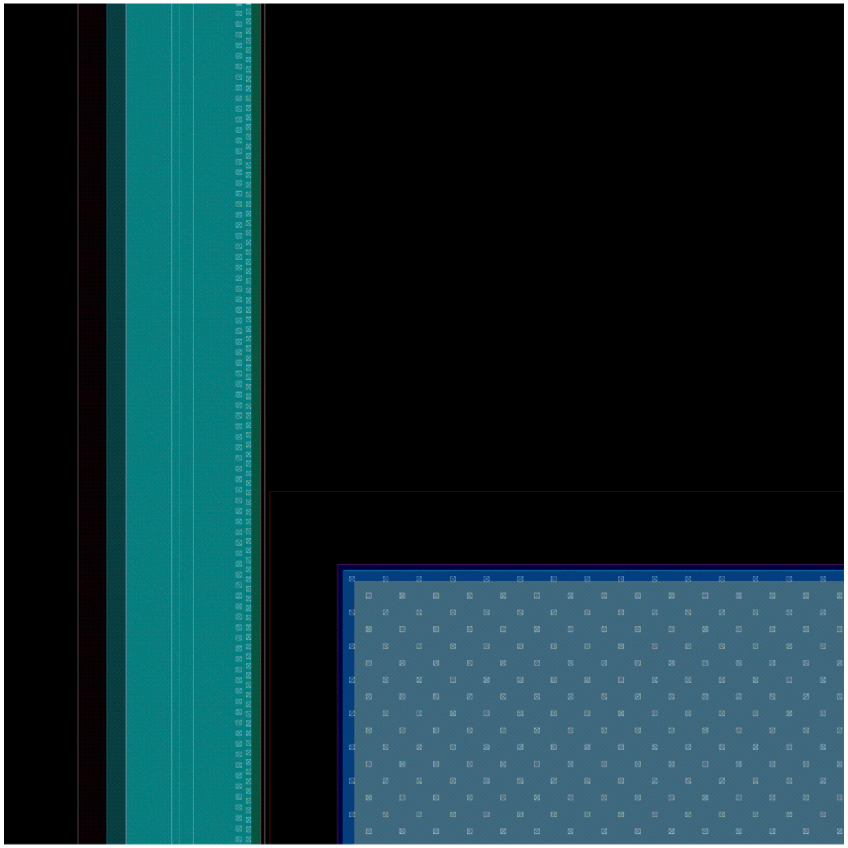
- ❑ Multiple busses provide clean/driver power
- ❑ VDD/GND pads drive the busses
- ❑ Output pads have protection circuitry and driver circuitry
- ❑ Input pads have protection circuitry
- ❑ Seal Ring
- ❑ Guard Rings

Bus Detail



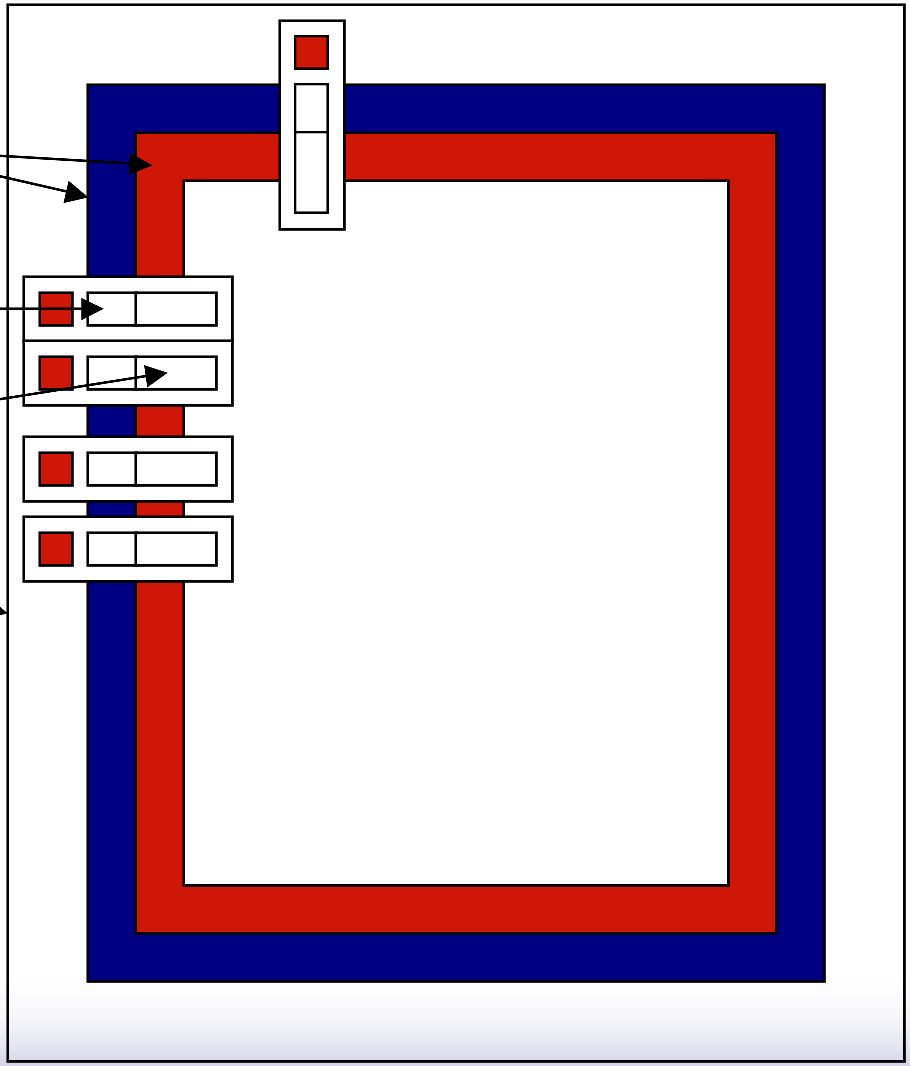
- ❑ Multiple supply rings simplify pad design
- ❑ Generic Layout Simplifies custom tuning
- ❑ Guard Rings Between sections of pad
- ❑ ESD/Driver
- ❑ Controller

Seal Ring



- Seal Ring is essentially a guard ring with metal layers and contacts placed to lower overglass to substrate evenly at chip boundary
- Hermetic seal of chip from atmosphere and other contamination

Pad Frame

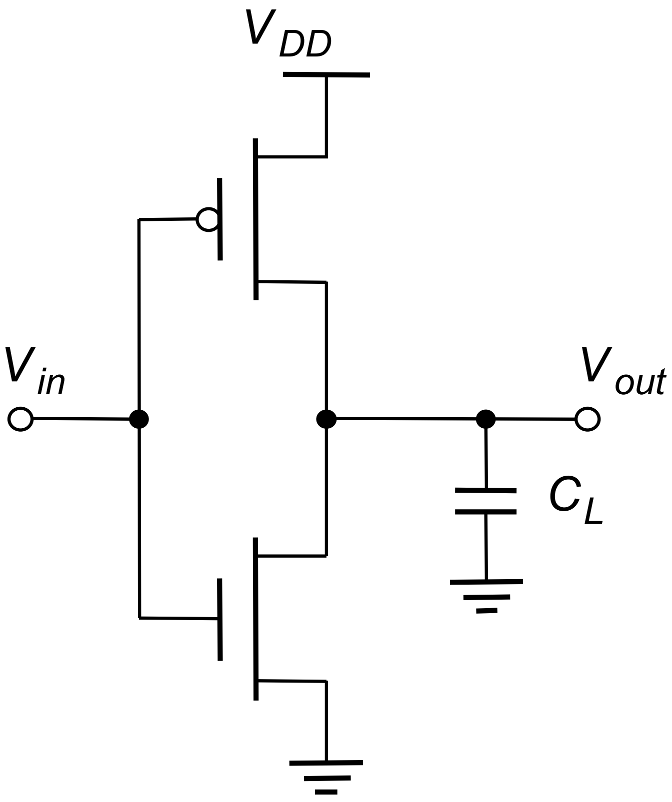


- Large Power Busses Surround Die
- ESD in PADS
- Driver/Logic in Pads
- Seal Ring
- Drive Bypass

Chip to Board Interface
-- Pad Design

- ❑ Buffer to drive PCB-scale parasitics
  - Capacitance 5-50pF, Impedance 30-90Ω
- ❑ Rise-Time Control
  - Noise injection to circuits and power supply
- ❑ ESD
  - Protection of chip-scale components
- ❑ Perimeter Pads/Area Bump

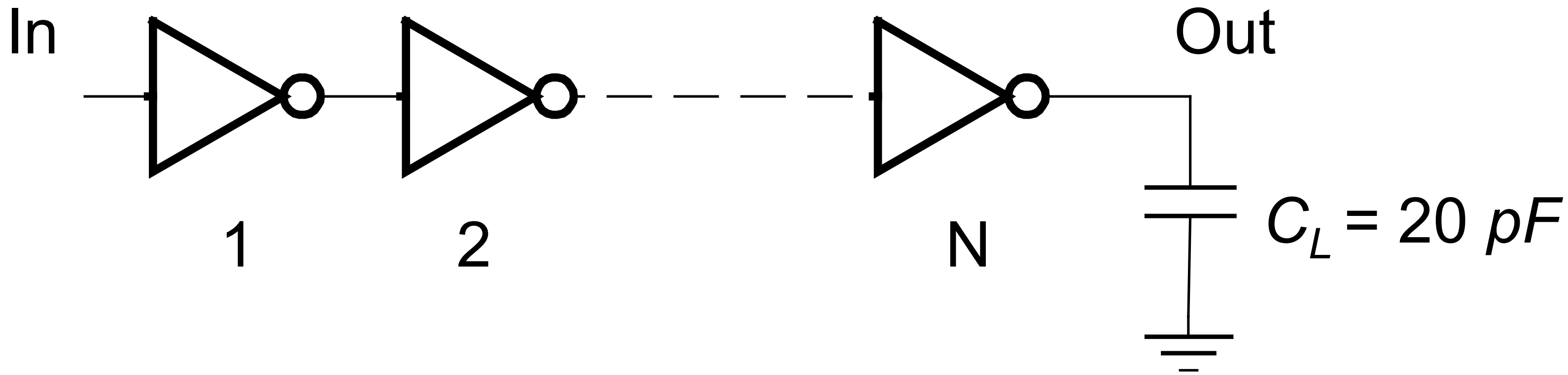
Driving Large Capacitances



$$\boxed{t_p = \frac{C_L V_{swing}}{I_{av}}}$$

- Transistor Sizing
- Cascaded Buffers

Using Cascaded Buffers



0.25 μm process
Cin* = 2.5 *fF
tp*0 = 30 *ps

***F* = *CL/Cin* = 8000**
***fopt* = 3.6 *N* = 7**
tp* = 0.76 *ns

(See Chapter 5)

Output Driver Design

Trade off Performance for Area and Energy

Given t_{pmax} find N and f

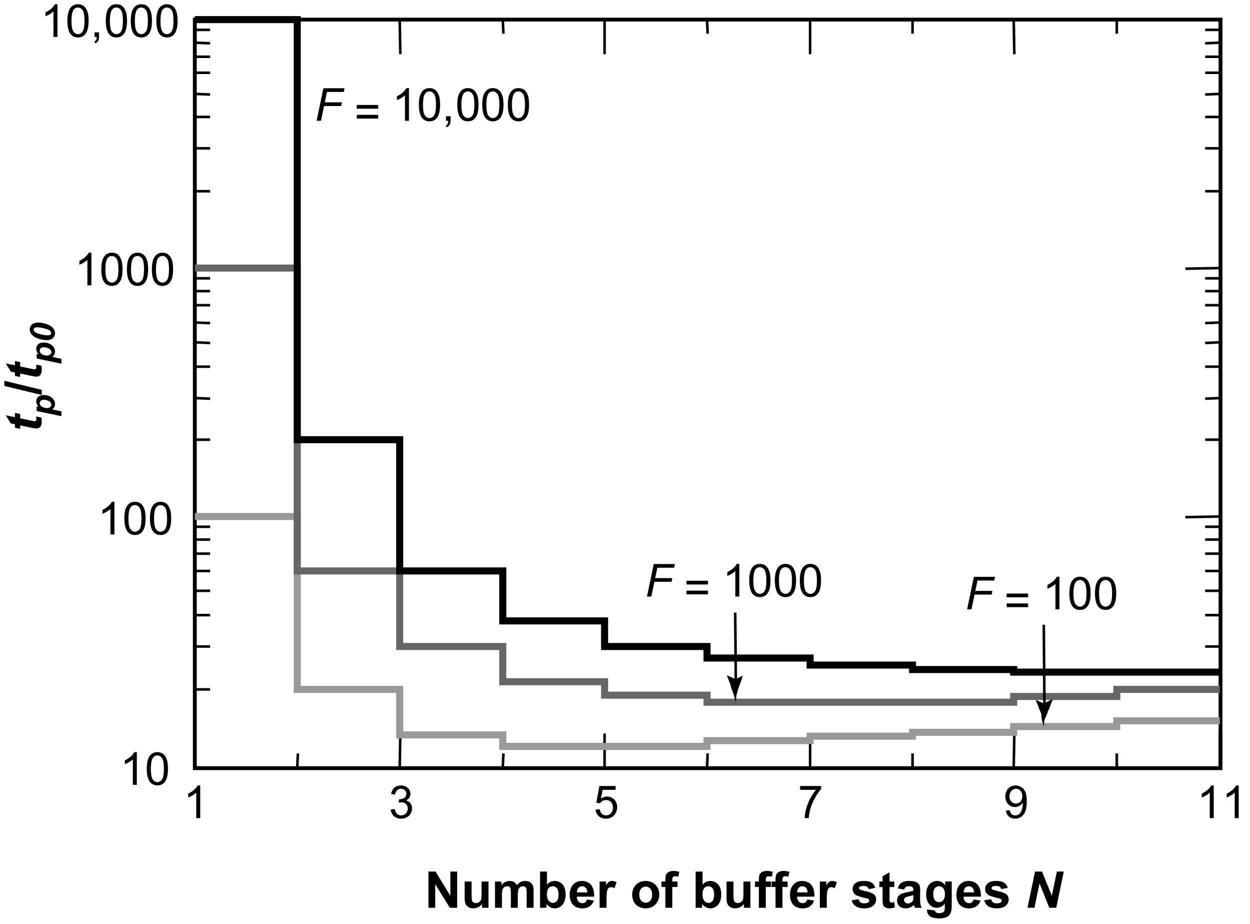
- Area

$$A_{driver} = \left(1 + f + f^2 + \ldots + f^{N-1}\right) A_{\min} = \frac{f^N - 1}{f - 1} A_{\min} = \frac{F - 1}{f - 1} A_{\min}$$

- Energy

$$E_{driver} = \left(1 + f + f^2 + \ldots + f^{N-1}\right) C_i V_{DD}^2 = \frac{F - 1}{f - 1} C_i V_{DD}^2 \approx \frac{C_L}{f - 1} V_{DD}^2$$

Delay as a Function of F and N



Output Driver Design

0.25 μm process, C_L = 20 *pF*

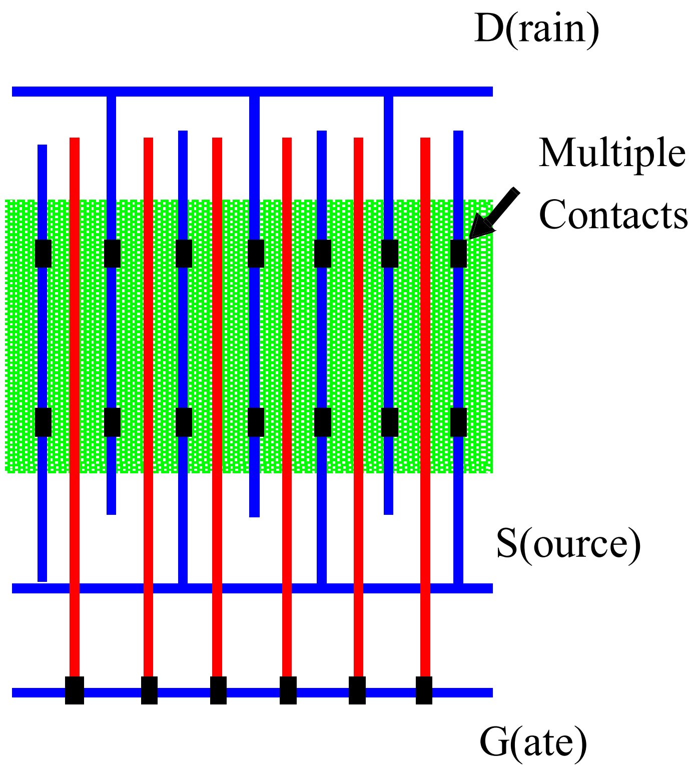
Transistor Sizes for optimally-sized cascaded buffer t_p = 0.76 *ns*

Stage	1	2	3	4	5	6	7
W_n (μm)	0.375	1.35	4.86	17.5	63	226.8	816.5
W_p (μm)	0.71	2.56	9.2	33.1	119.2	429.3	1545.5

Transistor Sizes of redesigned cascaded buffer t_p = 1.8 *ns*

Stage	1	2	3
W_n (μm)	0.375	7.5	150
W_p (μm)	0.71	14.4	284

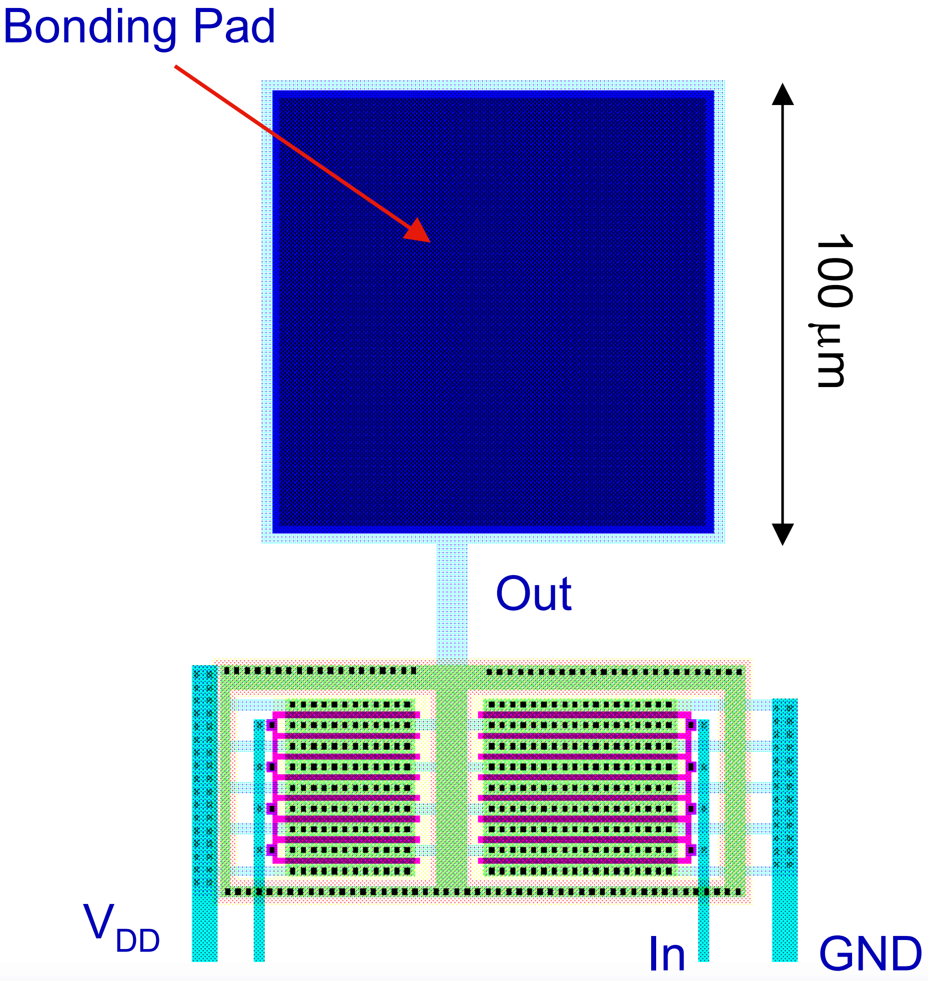
How to Design Large Transistors

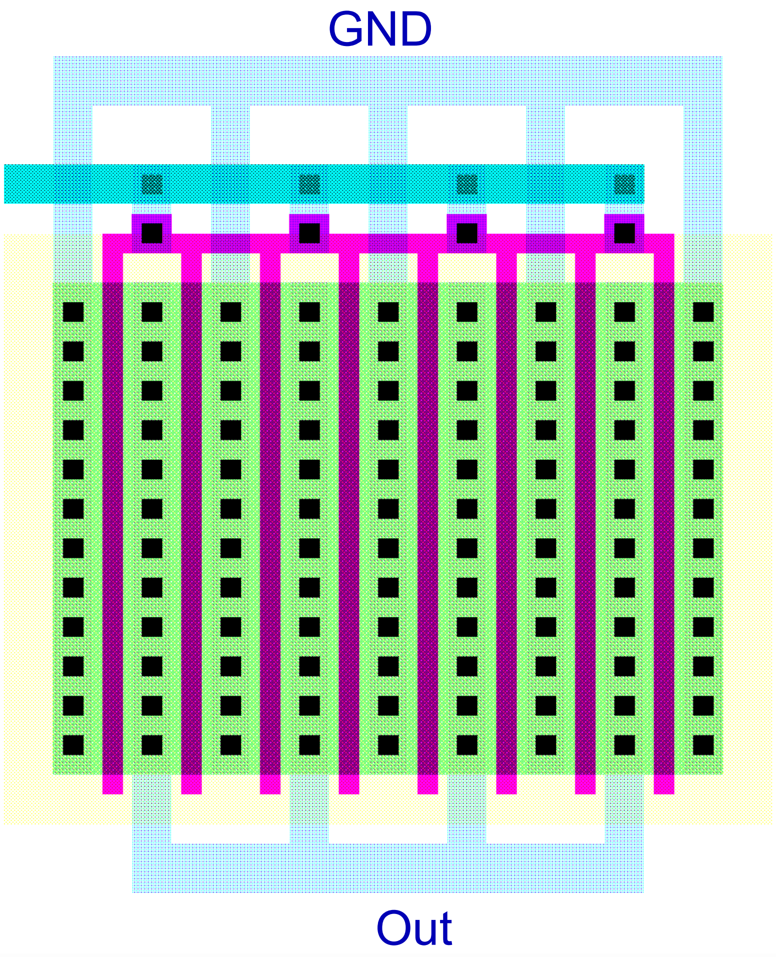


small transistors in parallel

Reduces diffusion capacitance
Reduces gate resistance

Bonding Pad Design

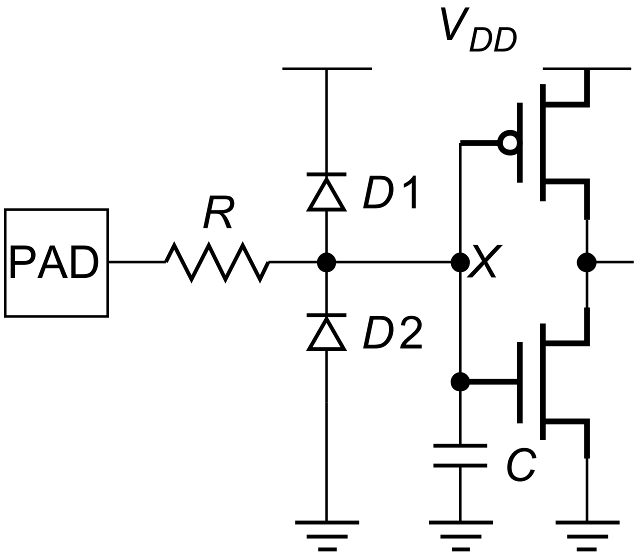


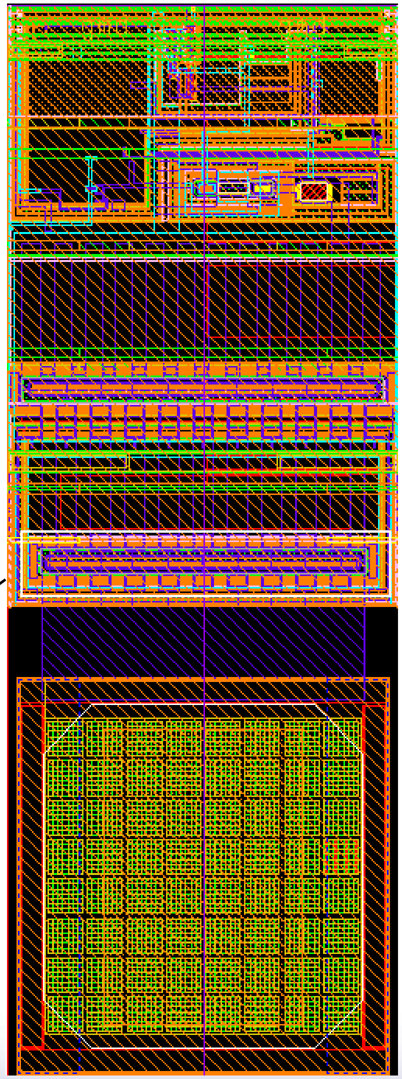


ESD Protection

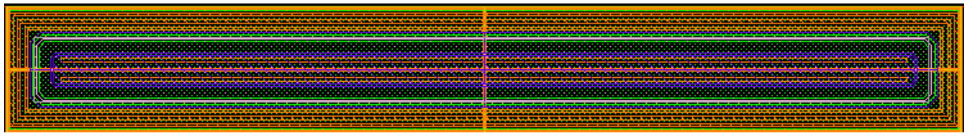
- When a chip is connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.

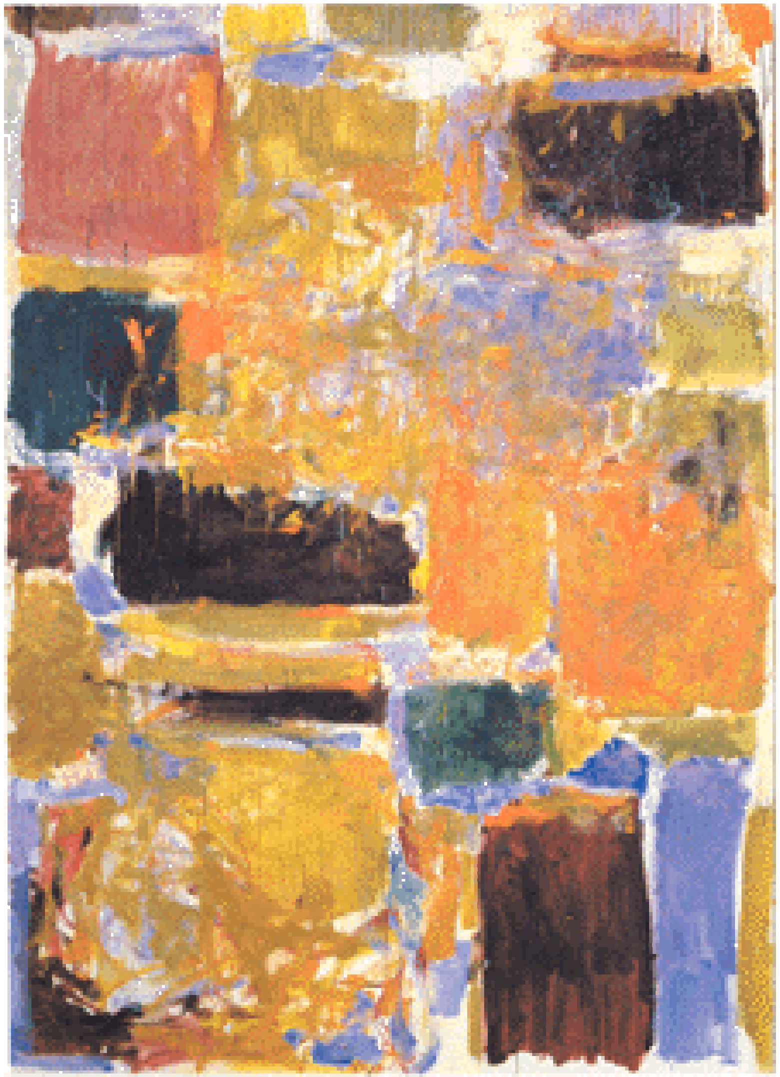
ESD Protection





Diode





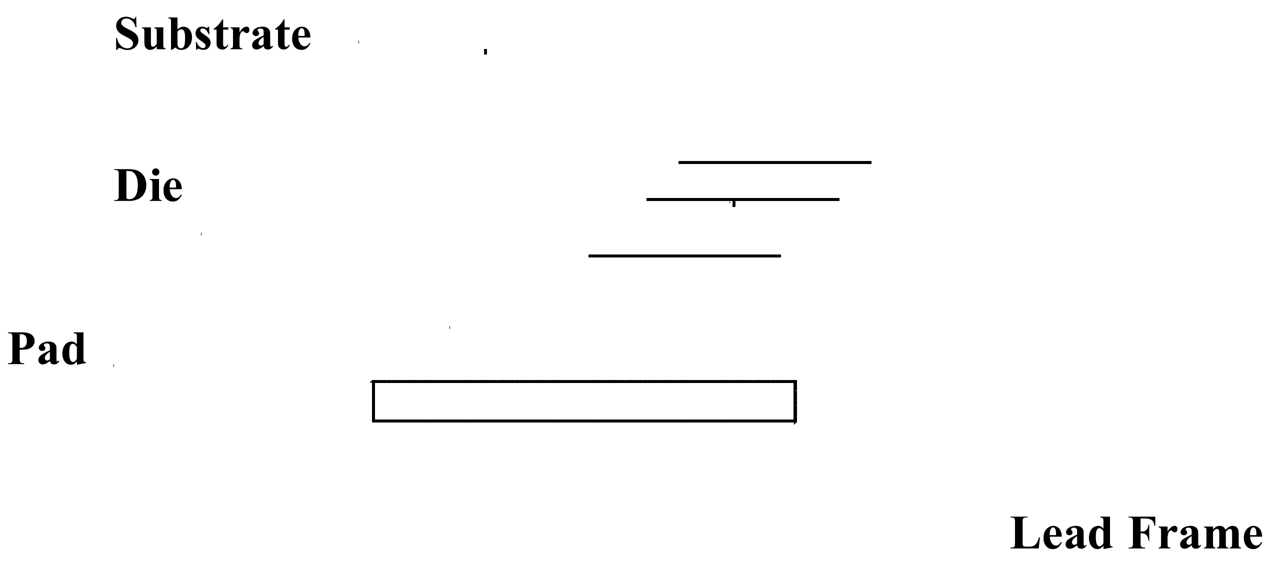
Packaging

Packaging Requirements

- ❑ Electrical: Low parasitics
- ❑ Mechanical: Reliable and robust
- ❑ Thermal: Efficient heat removal
- ❑ Economical: Cheap

Bonding Techniques

Wire Bonding



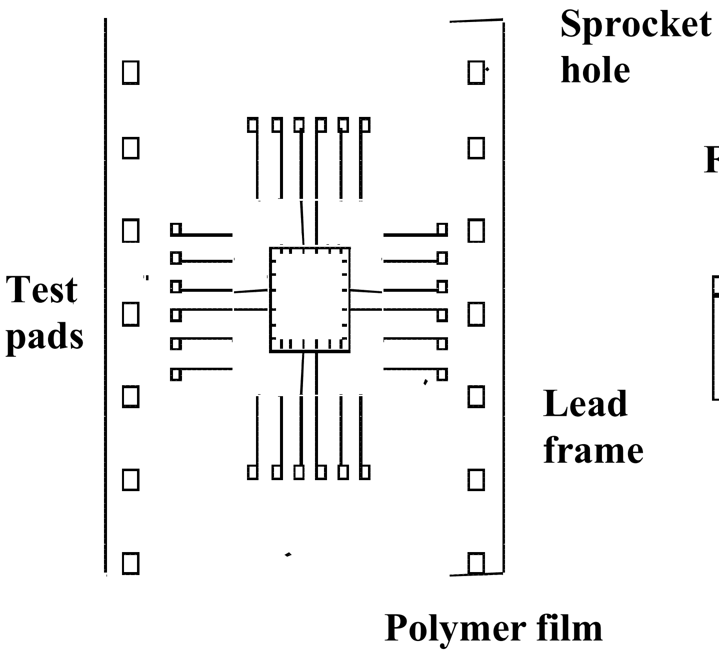
Substrate

Die

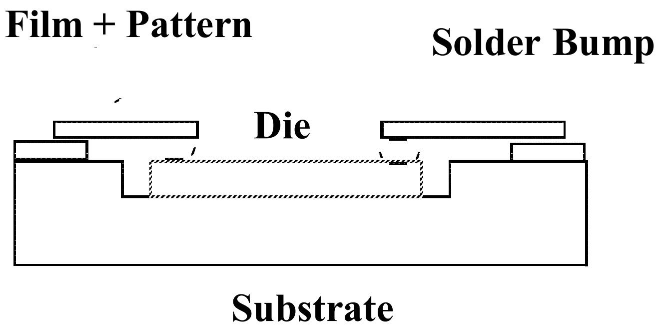
Pad

Lead Frame

Tape-Automated Bonding (TAB)

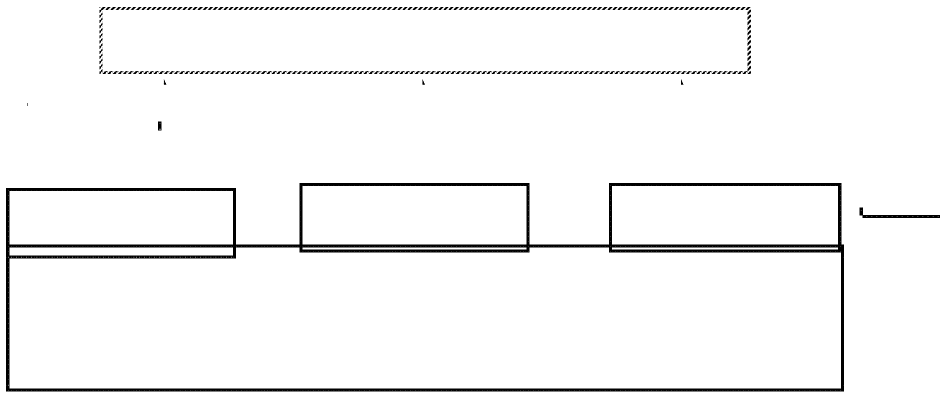


(a) Polymer Tape with imprinted wiring pattern.



(b) Die attachment using solder bumps.

Flip-Chip Bonding



Die

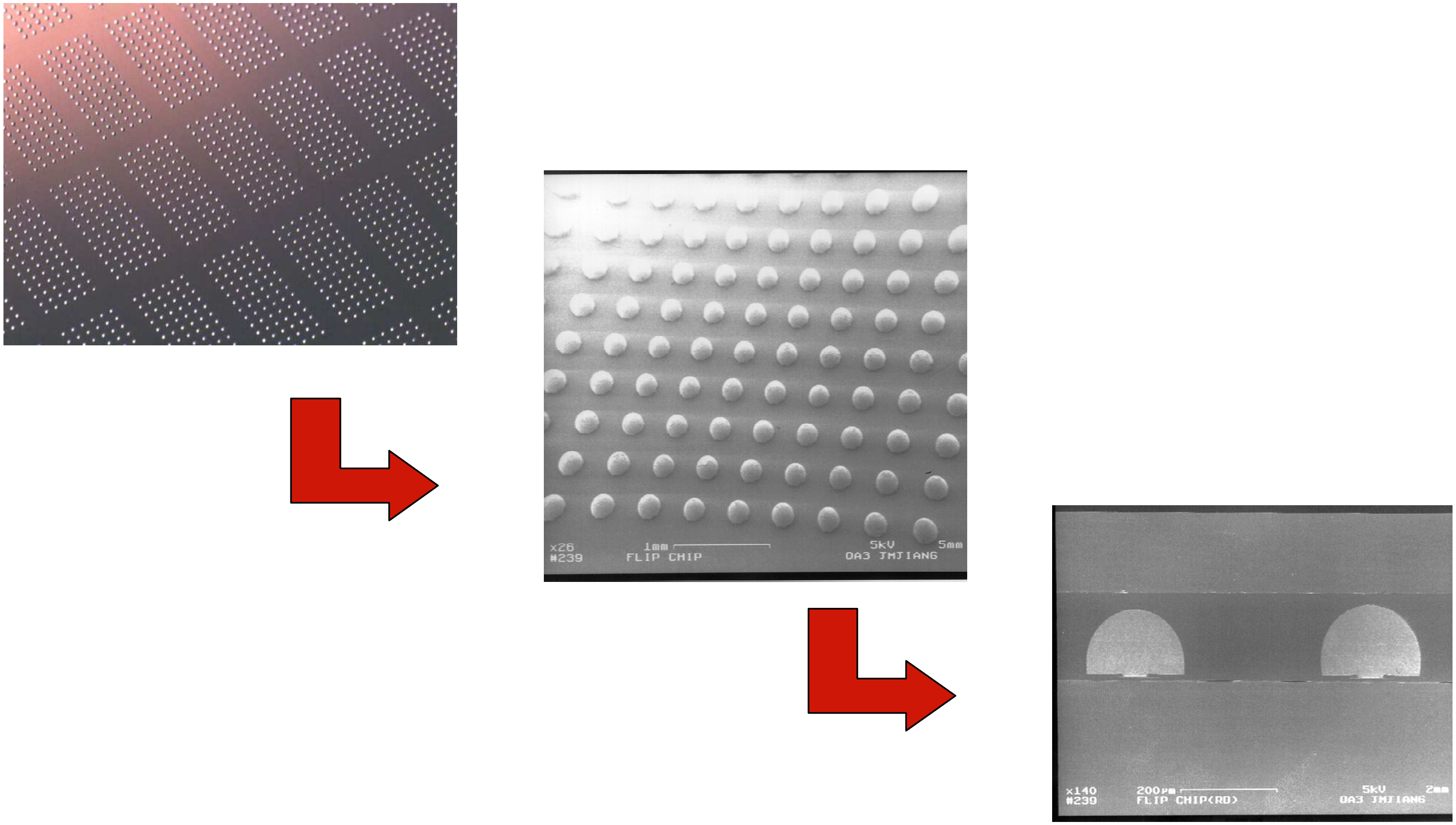
Solder bumps

Interconnect

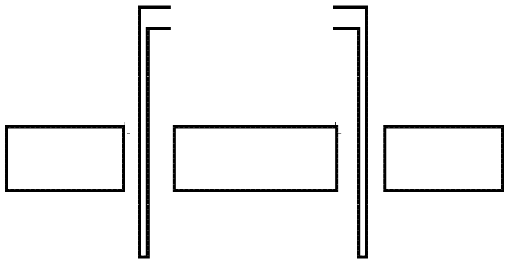
layers

Substrate

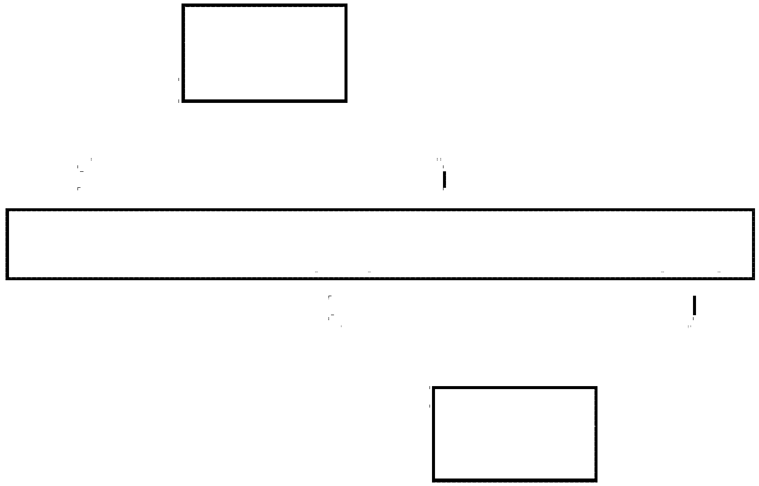
Cu Flip-Chip Technology



Package-to-Board Interconnect

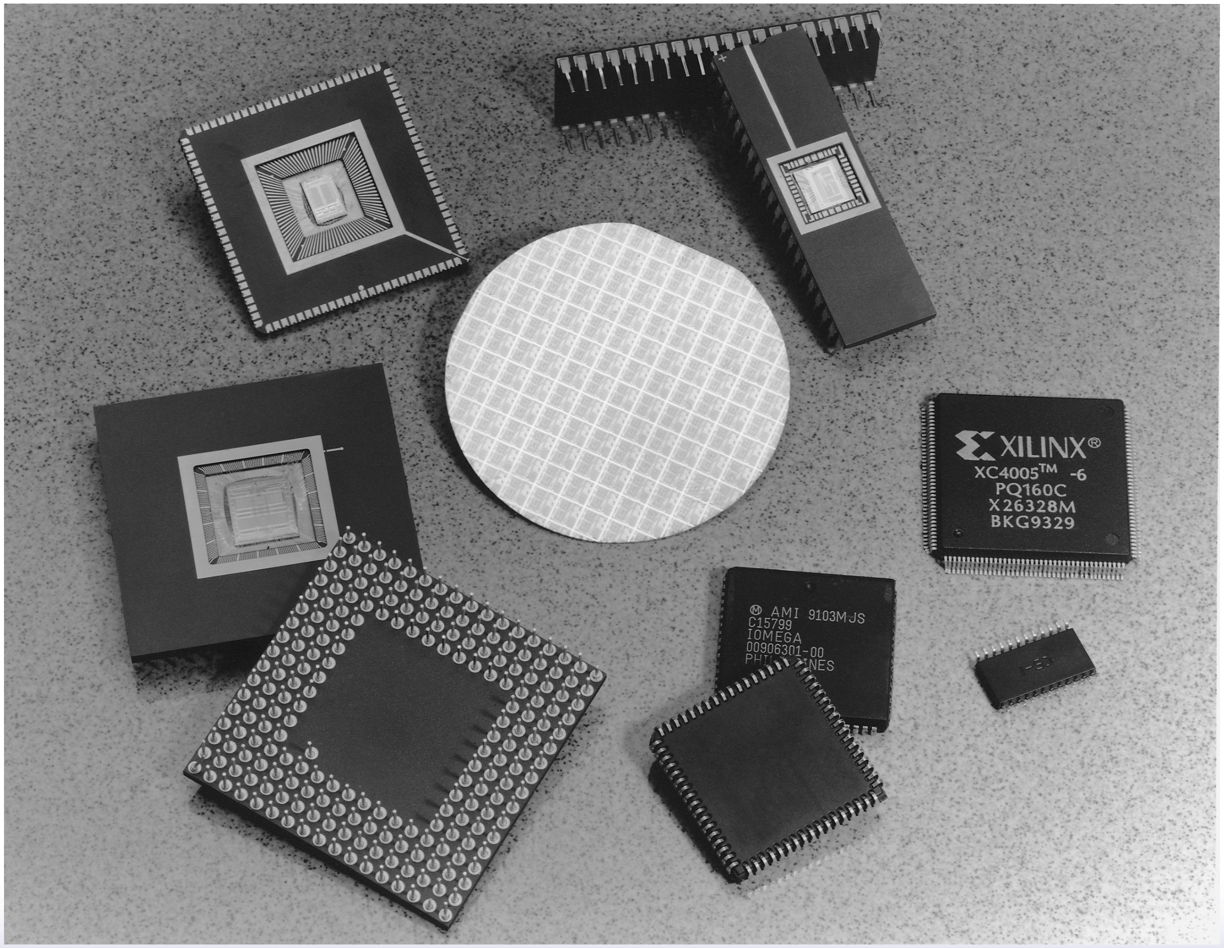


(a) Through-Hole Mounting

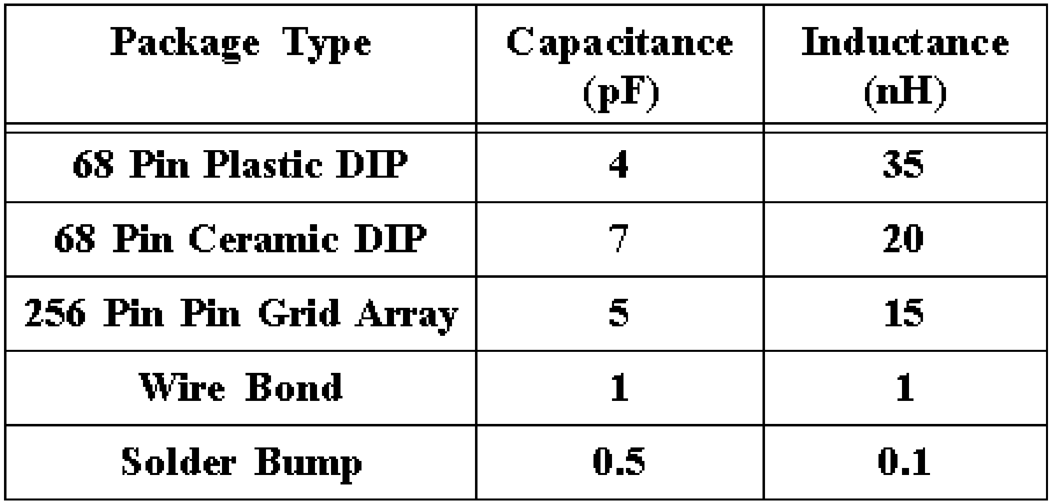


(b) Surface Mount

Package Types



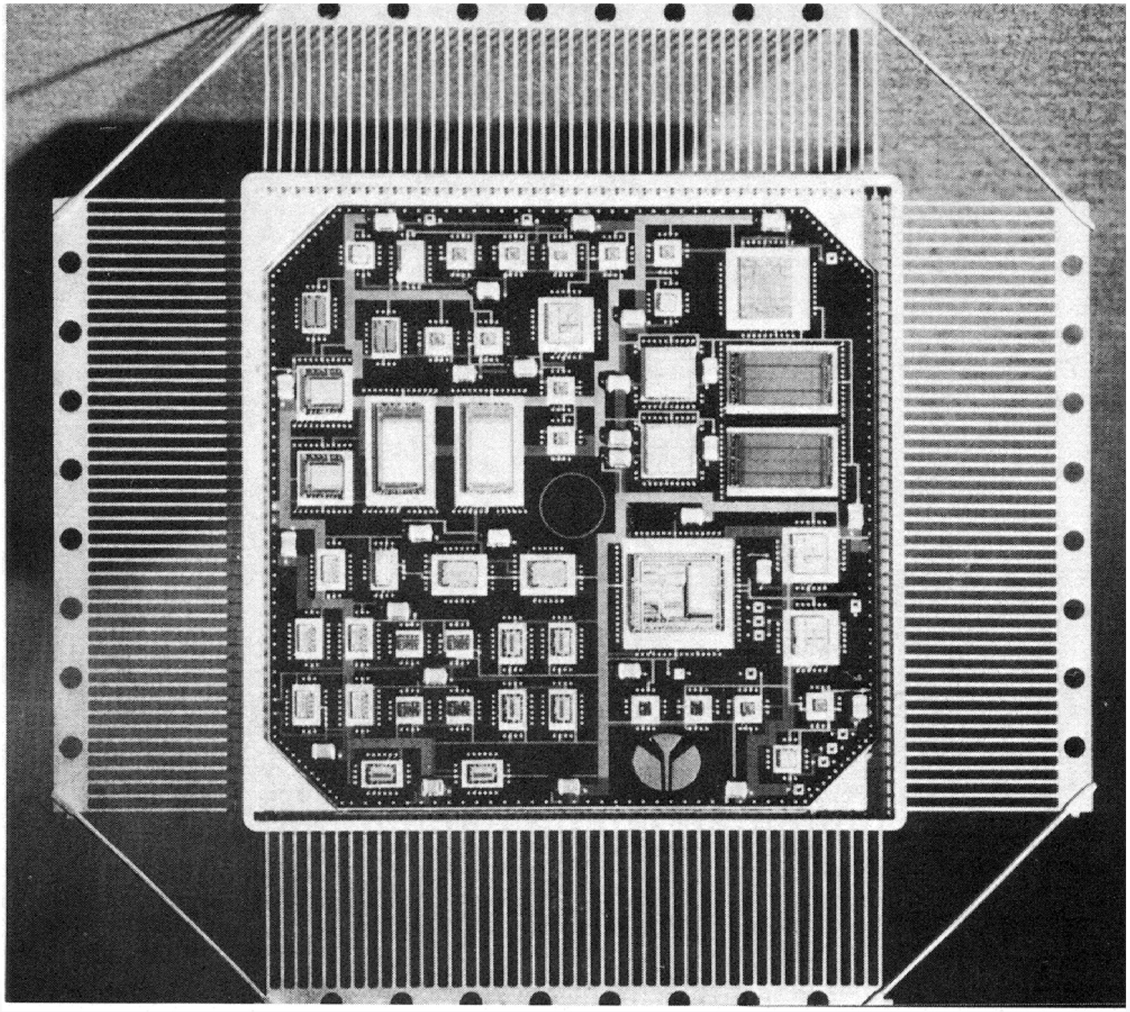
Package Parameters



Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Multi-Chip Modules



Lecture Problems 2

1. Why is there a spacing rule between via's and contacts and/or vias and other vias? How is it eliminated in deeper (smaller) processes?
2. Draw a schematic and stick layout for a 3-input 2-output adder cell (output is sum and carry). Design as two cells: a cell producing $\sim C_{out}$ and another cell producing $S_{out}(a,b,c,\sim C_{out})$. Design Sue schematics and Max Layout for the two cells with minimum size transistors and turn in check plots.
3. Guard Rings consist of n and p contact regions with continuous metal connections. They are often used to surround and isolate sensitive devices. How do they work?
4. Very wide metal (any layer) in most technologies needs to have slots cut in it. Why?
5. Explain the relation between CMP planarization and metal/poly density rules.
6. Draw schematics and stick layouts for a 2 of 4 majority gate (true if two or more of its inputs are False). Do two designs, one to minimize transistors, and one where the inputs arrive in order:a,b,c,d last ti minimize the critical path.