ECE 224a
Process and Design Rules

- Process Overview
- Device Fabrication Limits
- Derived Layers
- Self Alignment/Dual Damascene/CMP
- Design Rules
  - Resolution/Step Coverage/Process
  - Electrical/Reliability/Mechanical Stress
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
The Manufacturing Process

- Photo-Lithography
  - Mask to Resist
  - Resist to Pattern Layer
  - Process (Implant/Etch/Oxide/Nitride/…)
  - Cleanup (Clean/Planarization/Anneal)
  - Setup next Layer for Processing

For a great reference source:
http://www.reed-electronics.com/semiconductor
Photo-Lithographic Process

oxidation

photoresist removal (ashing)

photoresist coating

stepper exposure

Typical operations in a single photolithographic cycle (from [Fullman]).

process step

spin, rinse, dry

acid etch

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd ed.
Patterning of SiO₂

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

Chemical or plasma etch

(d) After development and etching of resist, chemical or plasma etch of SiO₂

(e) After etching

(f) Final result after removal of resist

CMOS Process Walk-Through

(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd
CMOS Process Walk-Through

(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{Tn}$ adjust implants

(f) After p-well and $V_{Tp}$ adjust implants

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd
CMOS Process Walk-Through

(g) After polysilicon deposition and etch

(h) After \( n^+ \) source/drain and \( p^+ \) source/drain implants. These steps also dope the polysilicon.

(i) After deposition of SiO\(_2\) insulator and contact hole etch.

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits\(^{2nd}\)
CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO insulator, etching of via’s, 2 deposition and patterning of second layer of Al.
# Advanced Process Modules

<table>
<thead>
<tr>
<th></th>
<th>Generation</th>
<th>Isolation</th>
<th>Substrate</th>
<th>Well</th>
<th>Gate Dielectric</th>
<th>Gate</th>
<th>Gate Litho</th>
<th>Junction Engineering</th>
<th>Silicide</th>
<th>BEOL Metal</th>
<th>BEOL Dielectric</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>0.25um</td>
<td>STI</td>
<td>Bulk/Epi</td>
<td>Retrograde --&gt; Advanced SSR</td>
<td>Multiple Gate Dielectric (Core/IO &amp; Mixed-Signal)</td>
<td>Dual Poly (n+/p+) Salicide</td>
<td>DUV 248nm</td>
<td>PSM</td>
<td>Advanced Junction/Pocket Engineering</td>
<td>CoSiX</td>
<td>Al</td>
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<tr>
<td></td>
<td>0.18um</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>193nm</td>
<td>PSM</td>
<td>TiSiX</td>
<td>Al and Cu</td>
<td>(K&lt;3.0)</td>
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<tr>
<td></td>
<td>0.15um</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>CoSiX</td>
<td>Cu</td>
<td>(K&lt;2.5)</td>
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<tr>
<td></td>
<td>0.13um</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NiSiX</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>0.1um</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition

Manufacturing
Lithography for 0.1um Node

80 nm Lines

120 nm Contact Holes

Poly Gate Etch ≤ 100nm

Experimental Simulation

Pre-trim
Trim X sec
Trim X+20 sec

Resist trimming is predictable by computer simulation as well as experiment.
12A Gate Oxide
Advanced Metallization

Dual damascene IC process

- Oxide deposition
- Stud lithography and reactive ion etch
- Wire lithography and reactive ion etch
- Stud and wire metal deposition
- Metal chemical-mechanical polish

Source: IBM Corp.

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition

Manufacturing
Interconnect RC Trend

- **Cu/Low-k1**
- **Al/Low-k1**

- 22% reduction
- 15% reduction

- **CL013**
- **CL015**
- **CL018**

**Technology**

- **RC delay is evaluated at minimum M2 pitch**

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
Design Rules

- What can be fabricated?
  - Resolution Limits
    - Light Source (357nm, 254nm, 193nm, ?)
    - Contact/Phase Masking
    - Surface State (Reflection/Scattering)
  - Material Limits
    - Step Coverage
    - Porosity/Defect Propagation
    - Mechanical/Thermal Stress
Design Rules II

- **Electrical Limits**
  - Electrical Fields (MV/cm)
  - Parasitic Conductivity/Devices (Latchup/ESD)
  - Joule Heating (Electro-Migration)

- **Defect Probability**
  - Contact/Via Replication
  - Grid-Based Power/Ground Networks

- **Advance Lithography**
  - Rule Explosion/Failure of Locality
  - CMP Area Rules/Antenna Rules
85nm Poly Gate Profile

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
## CL013 Core Device

<table>
<thead>
<tr>
<th>Technology</th>
<th>CL013LV (14 ps/gate* (</th>
<th>CL013G (20 ps/gate* (</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vcc</strong></td>
<td>1.0V NMOS</td>
<td>1.0V PMOS</td>
</tr>
<tr>
<td>Lg (um)</td>
<td>0.08</td>
<td>0.085</td>
</tr>
<tr>
<td>Idsat(uA/um)</td>
<td>610</td>
<td>260</td>
</tr>
<tr>
<td>Vt(V)</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Ioff(nA/um)**</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>BV(V)</td>
<td>&gt;2</td>
<td>&gt;2</td>
</tr>
</tbody>
</table>

* * Fanout = 1 ring oscillator
** * Room temp. & worst case.

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F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Manufacturing
## 0.13/0.18 Comparison

<table>
<thead>
<tr>
<th>Rule/Technology</th>
<th>CL018 1P6M</th>
<th>CL013 1P8M</th>
<th>Shrink Ratio(%) CL018 =&gt; CL013</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+/P+ spacing</td>
<td>0.86</td>
<td>0.62</td>
<td>72.0</td>
</tr>
<tr>
<td>OD (W/S)</td>
<td>0.22/0.28</td>
<td>0.15/0.21</td>
<td>72.0</td>
</tr>
<tr>
<td>Poly (W/S)</td>
<td>0.18/0.25</td>
<td>0.13/0.18</td>
<td>72.1</td>
</tr>
<tr>
<td>CO (W/S)</td>
<td>0.22/0.25</td>
<td>0.16/0.18</td>
<td>72.3</td>
</tr>
<tr>
<td>M1 (W/S)</td>
<td>0.23/0.23</td>
<td>0.16/0.18</td>
<td>73.9</td>
</tr>
<tr>
<td>Via1-Via (n-2) (W/S)</td>
<td>0.26/0.26</td>
<td>0.19/0.22</td>
<td>78.8</td>
</tr>
<tr>
<td>M2 ~ M(n-1) (W/S)</td>
<td>0.28/0.28</td>
<td>0.20/0.21</td>
<td>73.2</td>
</tr>
<tr>
<td>Via(n-1) (W/S)</td>
<td>0.36/0.35</td>
<td>0.36/0.35</td>
<td>100.0</td>
</tr>
<tr>
<td>Mn (W/S)</td>
<td>0.44/0.46</td>
<td>0.44/0.46</td>
<td>100.0</td>
</tr>
<tr>
<td>6T SRAM Cell (um²)</td>
<td>4.65</td>
<td>2.43</td>
<td>52.3</td>
</tr>
</tbody>
</table>

* Please refer to shrinkage guideline for non-shrinkable details

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F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits

Manufacturing
3D Perspective

[Diagram showing a 3D perspective of a semiconductor device with labels for Gate Oxide, Field Oxide, Polysilicon, Aluminum, Source/Drain Regions, and P-Type material.]

Poly-SiGe Gate
Design Rules III

- Interface twixt designer and process engineer
- Unit dimension: Minimum Feature Size
  - scalable design rules: lambda
  - absolute dimensions: (Vendor rules)
- Process Design Layers
  - Derived Layers
# CMOS Process Design Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td><img src="image" alt="Yellow Layer" /></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td><img src="image" alt="Green Layer" /></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td><img src="image" alt="Green Layer" /></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td><img src="image" alt="Red Layer" /></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td><img src="image" alt="Blue Layer" /></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td><img src="image" alt="Magenta Layer" /></td>
</tr>
<tr>
<td>Metal3</td>
<td>Gold</td>
<td><img src="image" alt="Gold Layer" /></td>
</tr>
<tr>
<td>Contact to poly/diff</td>
<td>Black</td>
<td><img src="image" alt="Black Layer" /></td>
</tr>
<tr>
<td>Vias</td>
<td>Black</td>
<td><img src="image" alt="Black Layer" /></td>
</tr>
</tbody>
</table>
Intra-Layer Design Rules

- **Well**: Same Potential (0 or 6), Different Potential (18)
  - 12 units

- **Active**: 3 units
  - Contact or Via Hole: 2 units

- **Select**: 2 units
  - Metal1/2: 3 units
  - Metal3: 5 units

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits

Manufacturing
3.1 FET length 2 (min)
3.2 FET spacing 3
3.3 Poly Overlap 2
3.4 Active Overlap 3
3.5 Space 1
Active Contact I

6.1 Size 2x2
6.2 Enclosure 1.5
6.3 Spacing 3
6.4 Space to FET 2

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
Poly Contact I

5.1 Size 2x2
5.2 Enclosure 1.5
5.3 Spacing 3
5.4 Space to FET 2

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
**Via (m1 to m2)**

9.1 Min Width 3  
9.2.a Spacing 3  
9.2.b Spacing 6 (width>10)  
9.3 Enclosure 1  

8.1 Size 2x2  
8.2 Spacing 3  
8.3 Enclosure 1  
8.4 Space to Contact 2  
8.5 Space to Poly/Act 2

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd
CMP Density Rules

- Chemical-Mechanical Polishing
  - Requires uniform density of metal/poly

- SCMOS Rules:
  - Poly 30% density across each 1mm² area
  - M1, M2 15% density
  - M3 (top metal) is not restricted since no further polishing...
Layout Guidelines I

- Group Transistors into Cells
  - Plan inter-cell wires first (Sticks)
  - Oversize Power Grids (Cell Default >6)
  - Frequent Substrate Contacts/Well Plugs
    - Every Well (even one will kill design!)
    - Max distance to plug/contact 5-8 microns

- Set a large user grid e.g. 1-2 lambda
  - Don’t optimize until you know the constraints
  - Plan for Change and Optimization
Electromigration (1)

Limits dc-current to 1 mA/μm

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition

Manufacturing
Electromigration (2)
Metal Migration

- **Al (2.9μΩcm M.P. 660 C)**
  - 1mA/μm² at 60C is average current limit for 10 year MTTF
  - Current density decreases rapidly with temperature

- **Cu (1.7μΩcm M.P. 1060 C)**
  - 10mA/μm² at 100C or better (depends on fabrication quality)
  - Density decreases with temperature, but much slower over practical Silicon operation temperatures <120C

- Find Average current through wire – check cross section
  - Be wary of Via's!! Typical cross section: 20-40% of
Layout Guidelines II

- Current Limits
  - 1 mA/μm² Avg. current limit (50C)
    - Strongly Temp Dependent (Al)
    - Failures typically occur at vias and contacts
    - Vias often Tungsten (higher resistance)
  - Wide Wires need via arrays!

- Transistor Contacts
  - Active is highly resistive
  - Avoid High Density Currents
Pads-- Chip to Board Interface

- Pads drive large Capacitances
  - 5pf minimum to much larger
  - Rise time control
- Board Impedance and Noise
  - L dl/dt Noise
- Coupling to Power Distribution
- ESD
Chip Packaging

- Bond wires (~25μm) are used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large (~100μm in 0.25μm technology), with large pitch (100μm)
- Many chips areas are ‘pad limited’
Pad Frame

Layout

Die Photo

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits2nd

Manufacturing
Pad Example

- Multiple busses provide clean/driver power
- VDD/GND pads drive the busses
- Output pads have protection circuitry and driver circuitry
- Input pads have protection circuitry
- Seal Ring
- Guard Rings

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Bus Detail

- Multiple supply rings simplify pad design
- Generic Layout Simplifies custom tuning
- Guard Rings Between sections of pad
- ESD/Driver
- Controller

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Seal Ring

- Seal Ring is essentially a guard ring with metal layers and contacts placed to lower overglass to substrate evenly at chip boundary
- Hermetic seal of chip from atmosphere and other contamination
Pad Frame

- Large Power Busses Surround Die
- ESD in PADS
- Driver/Logic in Pads
- Seal Ring
- Drive Bypass

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd
Manufacturing
Chip to Board Interface
-- Pad Design

- Buffer to drive PCB-scale parasitics
  - Capacitance 5-50pF, Impedance 30-90Ω
- Rise-Time Control
  - Noise injection to circuits and power supply
- ESD
  - Protection of chip-scale components
- Perimeter Pads/Area Bump
Driving Large Capacitances

\[ t_p = \frac{C_L V_{\text{swing}}}{I_{av}} \]

- Transistor Sizing
- Cascaded Buffers

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Using Cascaded Buffers

(See Chapter 5)

0.25 \text{ \mu m} \text{ process}

\begin{align*}
C_{in} &= 2.5 \text{ fF} \\
\tau p_0 &= 30 \text{ ps}
\end{align*}

\begin{align*}
F &= \frac{C_L}{C_{in}} = 8000 \\
\tau opt &= 3.6 \quad N = 7 \\
\tau p &= 0.76 \text{ ns}
\end{align*}

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits$^{2nd}$ Manufacturing
Output Driver Design

Trade off Performance for Area and Energy

Given \( t_{pmax} \) find \( N \) and \( f \)

- **Area**

  \[ A_{driver} = \left(1 + f + f^2 + \ldots + f^{N-1}\right) A_{min} = \frac{f^N - 1}{f - 1} A_{min} = \frac{F - 1}{f - 1} A_{min} \]

- **Energy**

  \[ E_{driver} = \left(1 + f + f^2 + \ldots + f^{N-1}\right) C_i V_{DD}^2 = \frac{F - 1}{f - 1} C_i V_{DD}^2 \approx \frac{C_L}{f - 1} V_{DD}^2 \]
Delay as a Function of F and N

![Graph showing the delay as a function of F and N. The x-axis represents the number of buffer stages N, and the y-axis represents t_p/t_{p0}. There are three curves for different values of F: F = 10,000, F = 1000, and F = 100. The graph illustrates the increase in delay with the number of buffer stages and the effect of different F values.]
### Output Driver Design

0.25 μm process, $C_L = 20 \, pF$

Transistor Sizes for optimally-sized cascaded buffer $t_p = 0.76 \, ns$

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n$ (μm)</td>
<td>0.375</td>
<td>1.35</td>
<td>4.86</td>
<td>17.5</td>
<td>63</td>
<td>226.8</td>
<td>816.5</td>
</tr>
<tr>
<td>$W_p$ (μm)</td>
<td>0.71</td>
<td>2.56</td>
<td>9.2</td>
<td>33.1</td>
<td>119.2</td>
<td>429.3</td>
<td>1545.5</td>
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</table>

Transistor Sizes of redesigned cascaded buffer $t_p = 1.8 \, ns$

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n$ (μm)</td>
<td>0.375</td>
<td>7.5</td>
<td>150</td>
</tr>
<tr>
<td>$W_p$ (μm)</td>
<td>0.71</td>
<td>14.4</td>
<td>284</td>
</tr>
</tbody>
</table>
How to Design Large Transistors

- Reduces diffusion capacitance
- Reduces gate resistance

Small transistors in parallel

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
Bonding Pad Design

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd

Manufacturing
ESD Protection

- When a chip is connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.
ESD Protection

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits

Manufacturing
Packaging
Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap
Bonding Techniques

Wire Bonding

Substrate

Die

Pad

Lead Frame

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**Tape-Automated Bonding (TAB)**

(a) Polymer Tape with imprinted wiring pattern.

(b) Die attachment using solder bumps.

Sprocket hole

Test pads

Lead frame

Polymer film

Film + Pattern

Die

Solder Bump

Substrate

Flip-Chip Bonding

Die

Solder bumps

Interconnect layers

Substrate
Cu Flip-Chip Technology

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits$^{2nd}$ Manufacturing
Package-to-Board Interconnect

(a) Through-Hole Mounting  (b) Surface Mount

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits 2nd Edition
Package Types
## Package Parameters

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Capacitance (pF)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68 Pin Plastic DIP</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>68 Pin Ceramic DIP</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>256 Pin Pin Grid Array</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Solder Bump</td>
<td>0.5</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits$^{2nd}$ Manufacturing
Multi-Chip Modules

F. Brewer, adapted from MOSIS Data, Digital Integrated Circuits2nd

Manufacturing
Lecture Problems 2

1. Why is there a spacing rule between via’s and contacts and/or vias and other vias? How is it eliminated in deeper (smaller) processes?

2. Draw a schematic and stick layout for a 3-input 2-output adder cell (output is sum and carry). Design as two cells: a cell producing \( \sim C_{out} \) and another cell producing \( S_{out}(a, b, c, \sim C_{out}) \). Design Sue schematics and Max Layout for the two cells with minimum size transistors and turn in check plots.

3. Guard Rings consist of n and p contact regions with continuous metal connections. They are often used to surround and isolate sensitive devices. How do they work?

4. Very wide metal (any layer) in most technologies needs to have slots cut in it. Why?

5. Explain the relation between CMP planarization and metal/poly density rules.

6. Draw schematics and stick layouts for a 2 of 4 majority gate (true if two or more of its inputs are False). Do two designs, one to minimize transistors, and one where the inputs arrive in order: a, b, c, d last to minimize the critical path.