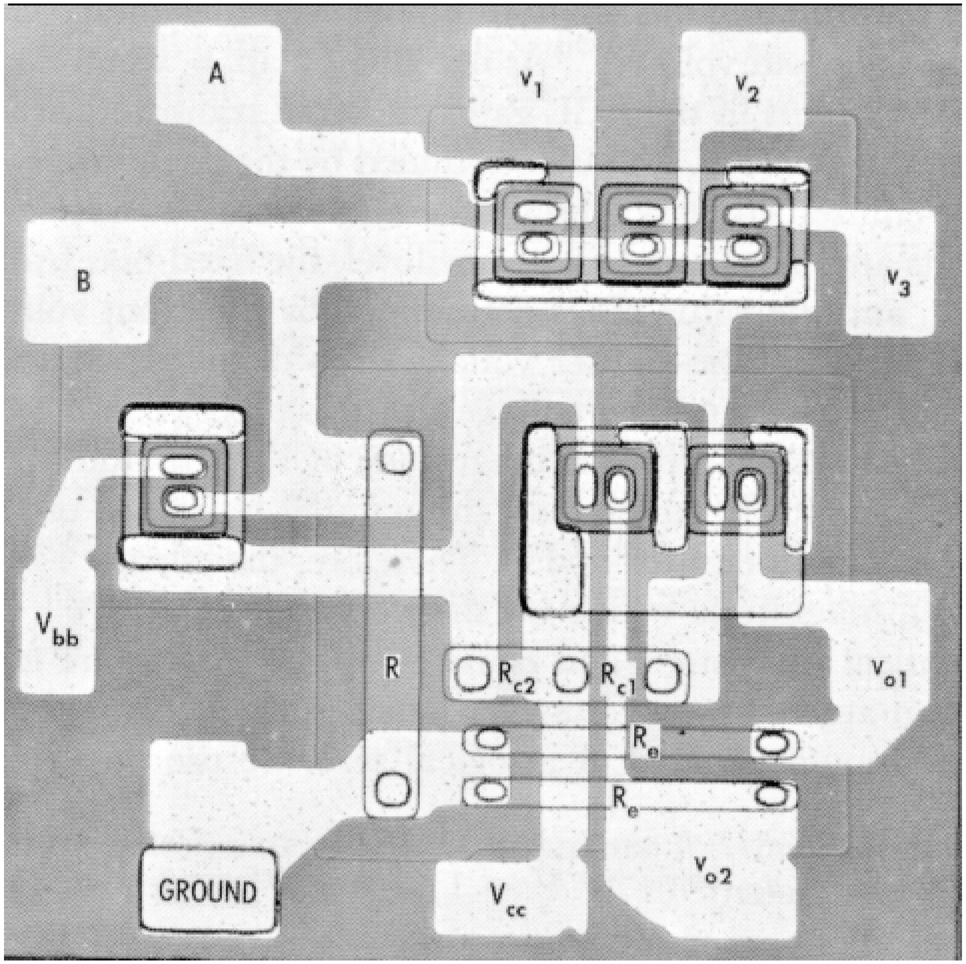
ECE 224a Lecture 1

- ❑ Moore's Law
- ❑ Design Cost/Yield
- ❑ Power Overview
- ❑ Logic Properties

Slides Adapted from: 2/e
Digital Integrated Circuits

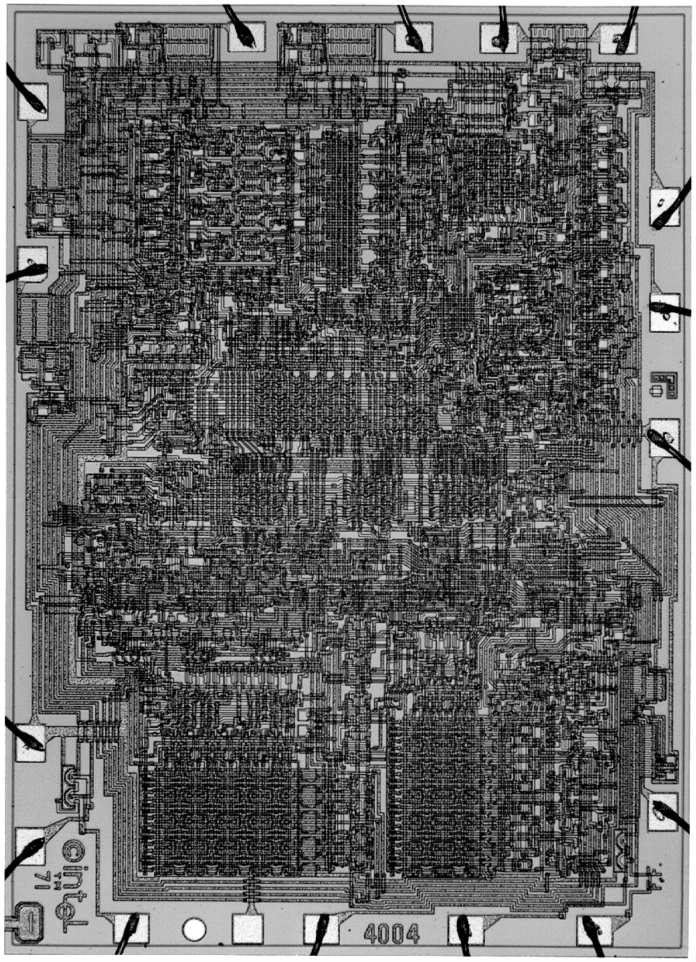
The First Integrated Circuits



Bipolar logic
1960's

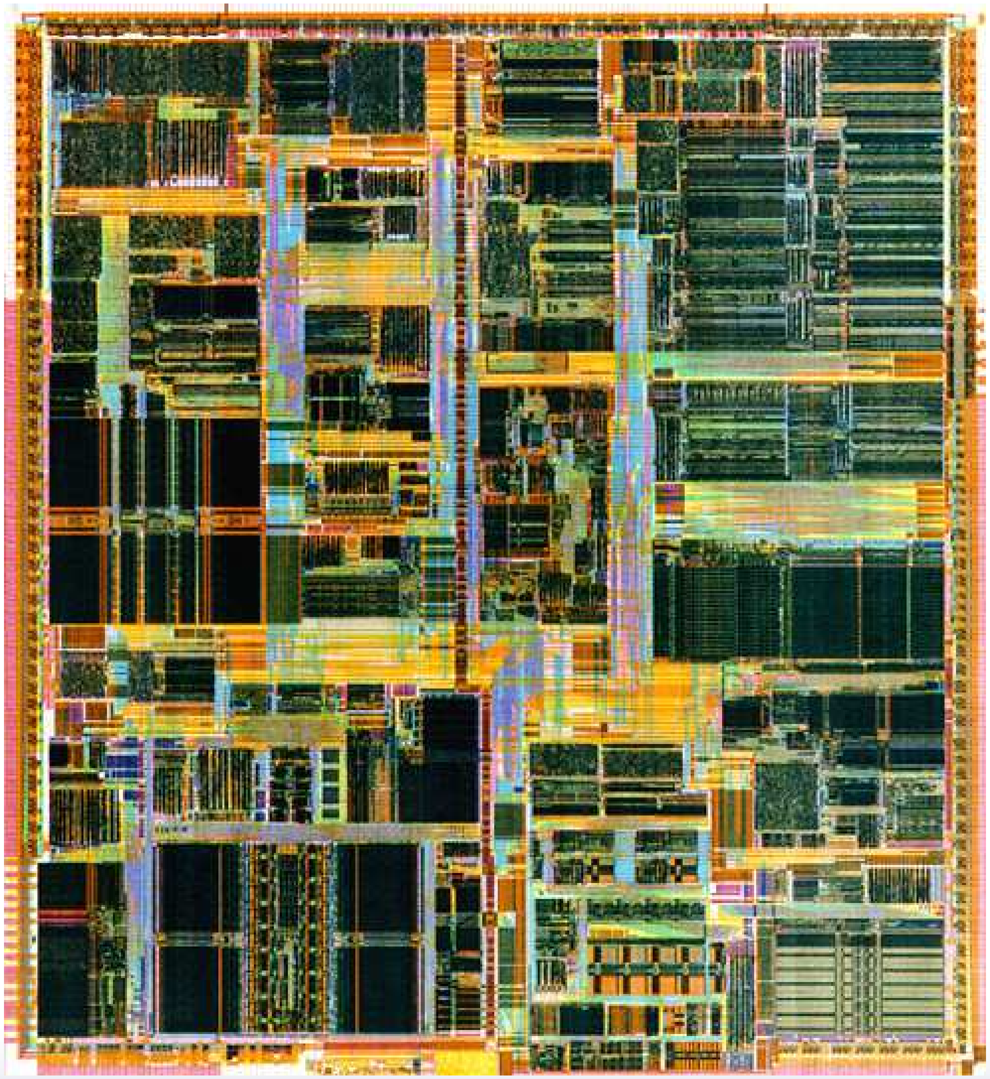
ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation

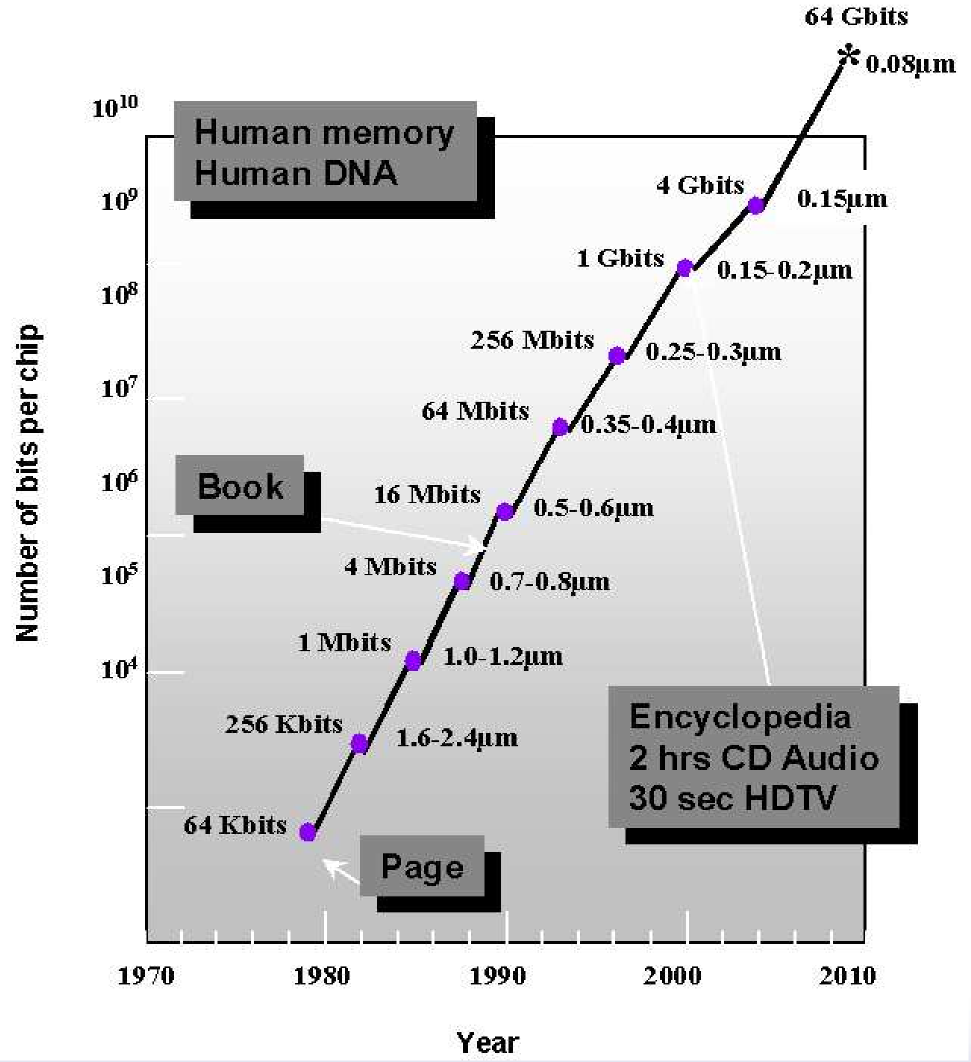
Intel Pentium (IV) microprocessor



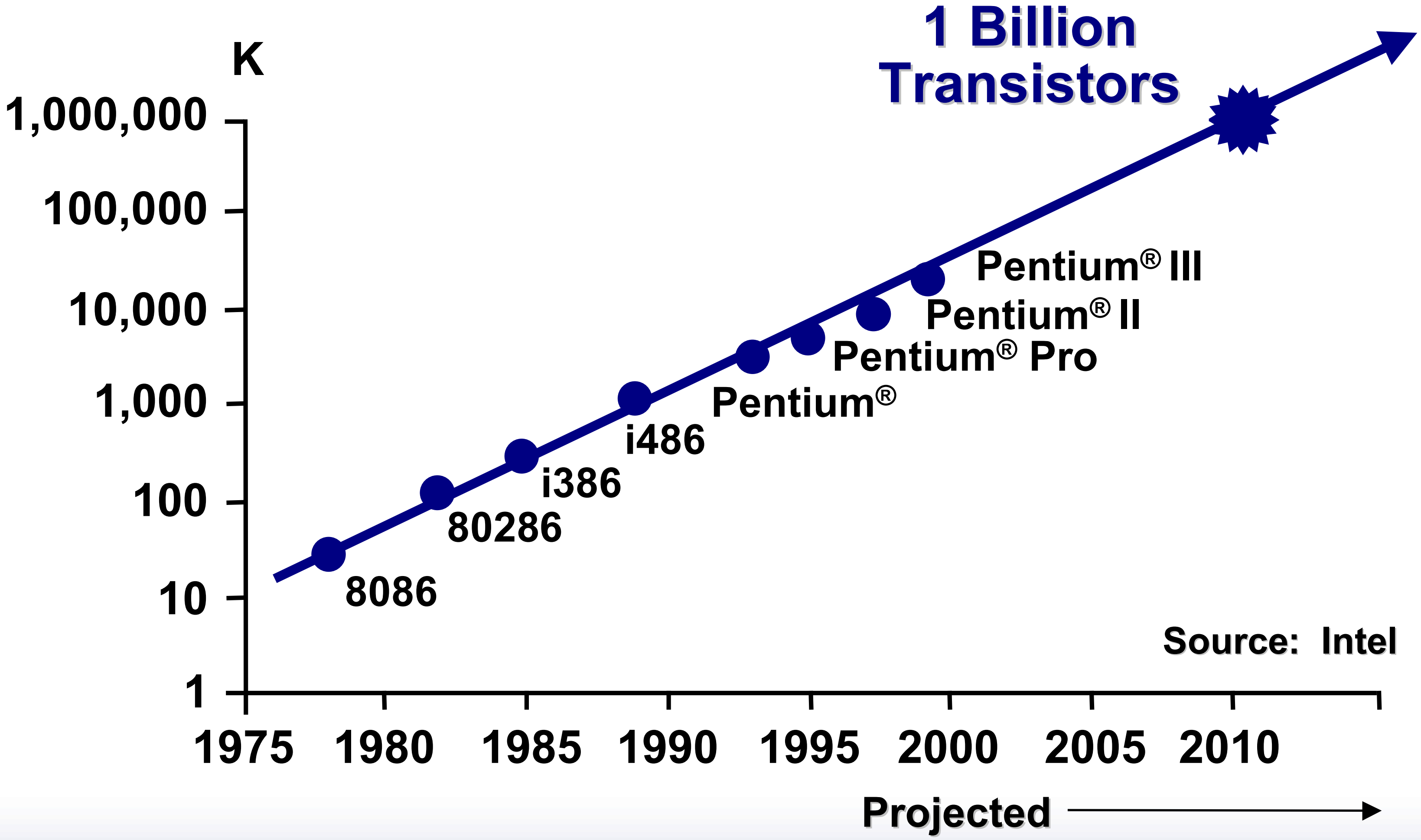
Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months
- Became industry maxim
- Physical constraints limit future growth

Evolution in Complexity

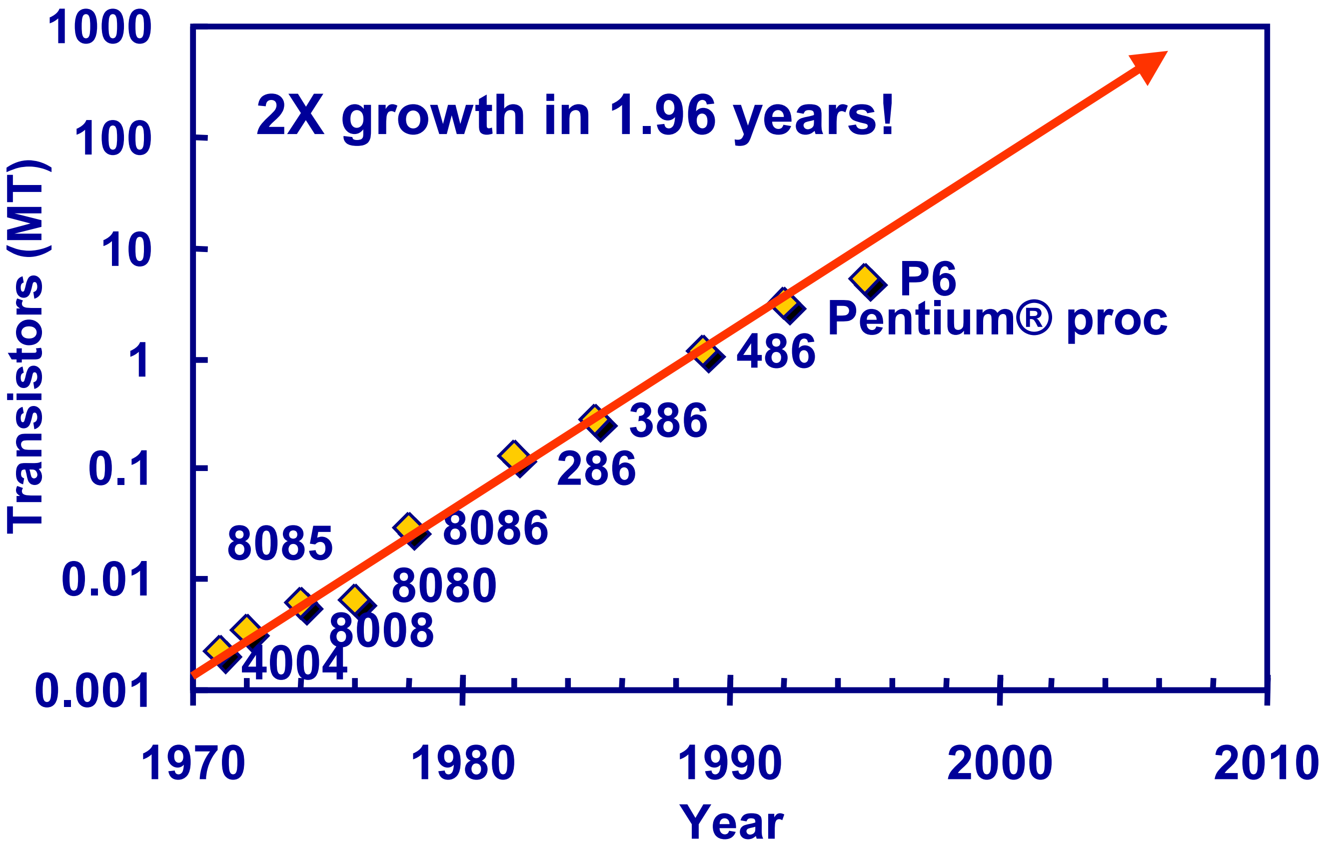


Transistor Counts

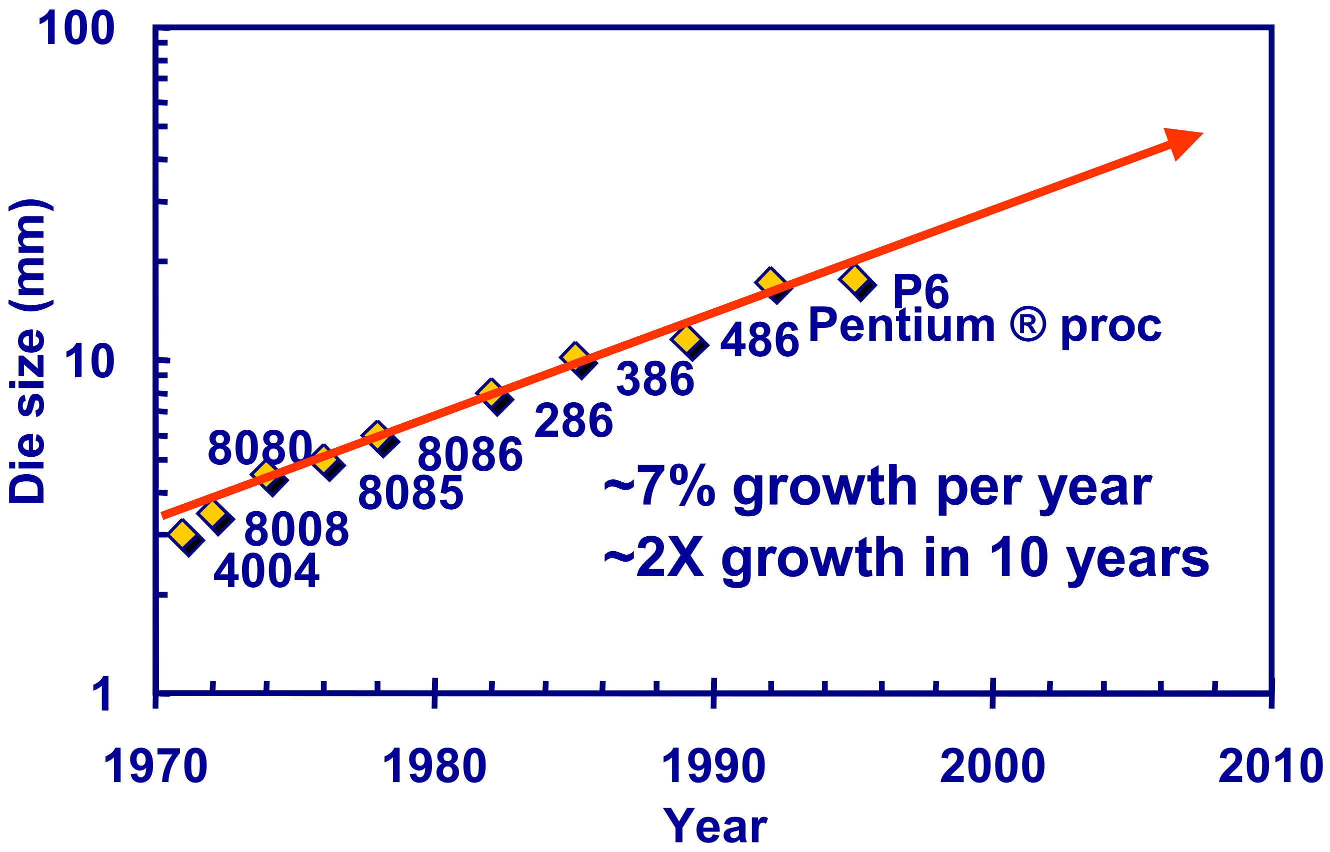


Courtesy, Intel

Moore’s law in Microprocessors



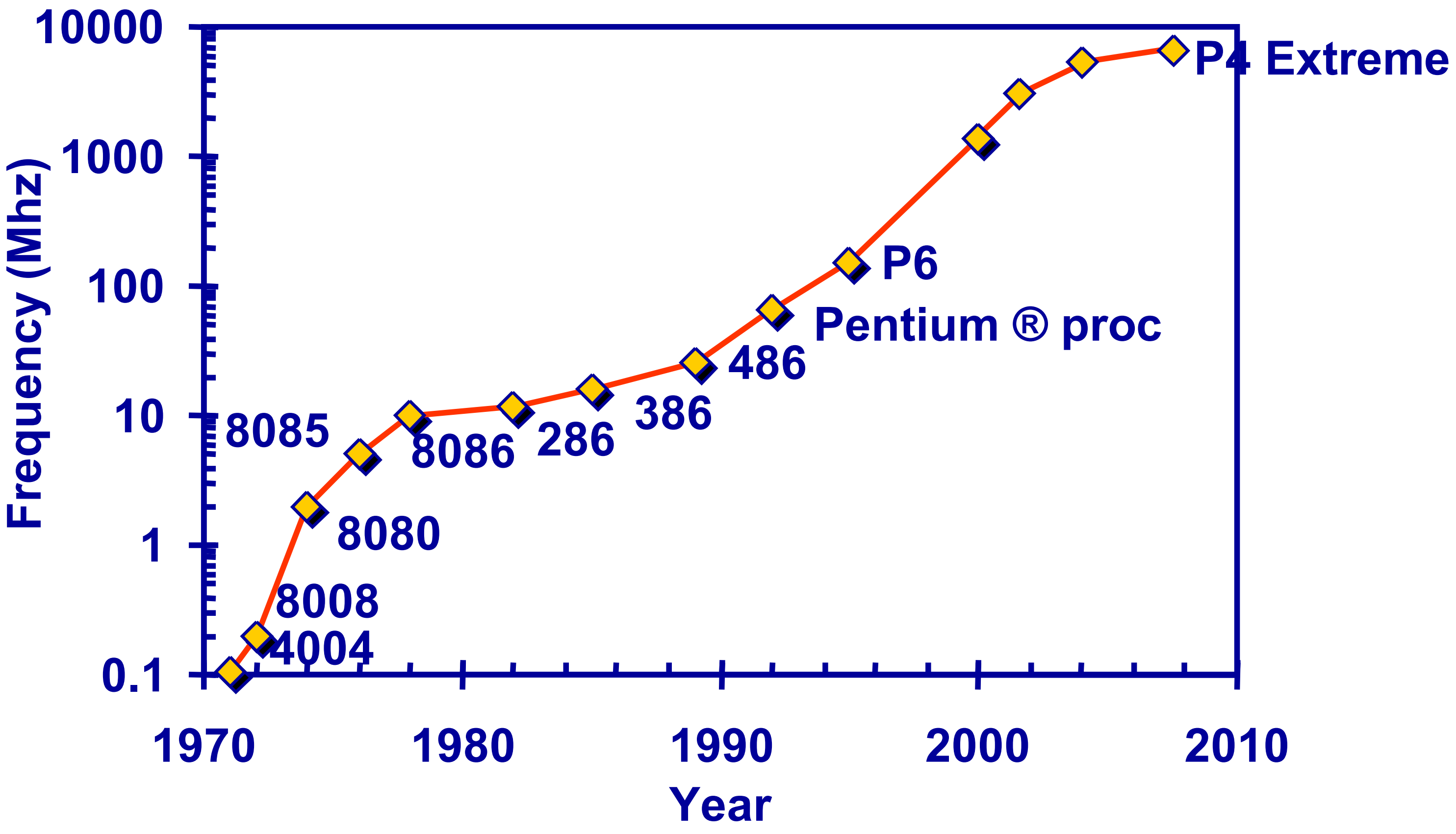
Die Size Growth



Die size grows by 14% to satisfy Moore's Law

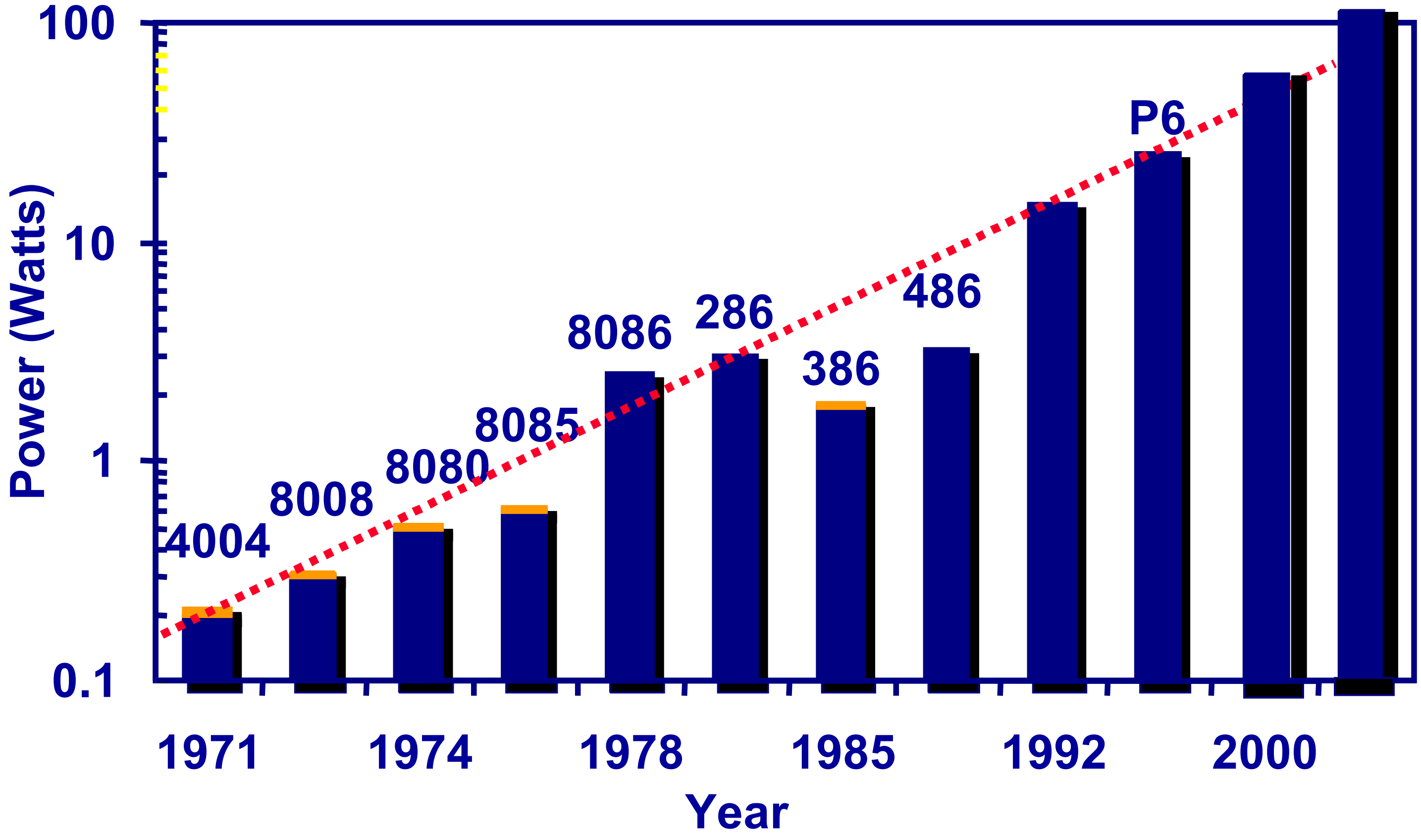
Courtesy, Intel

Frequency



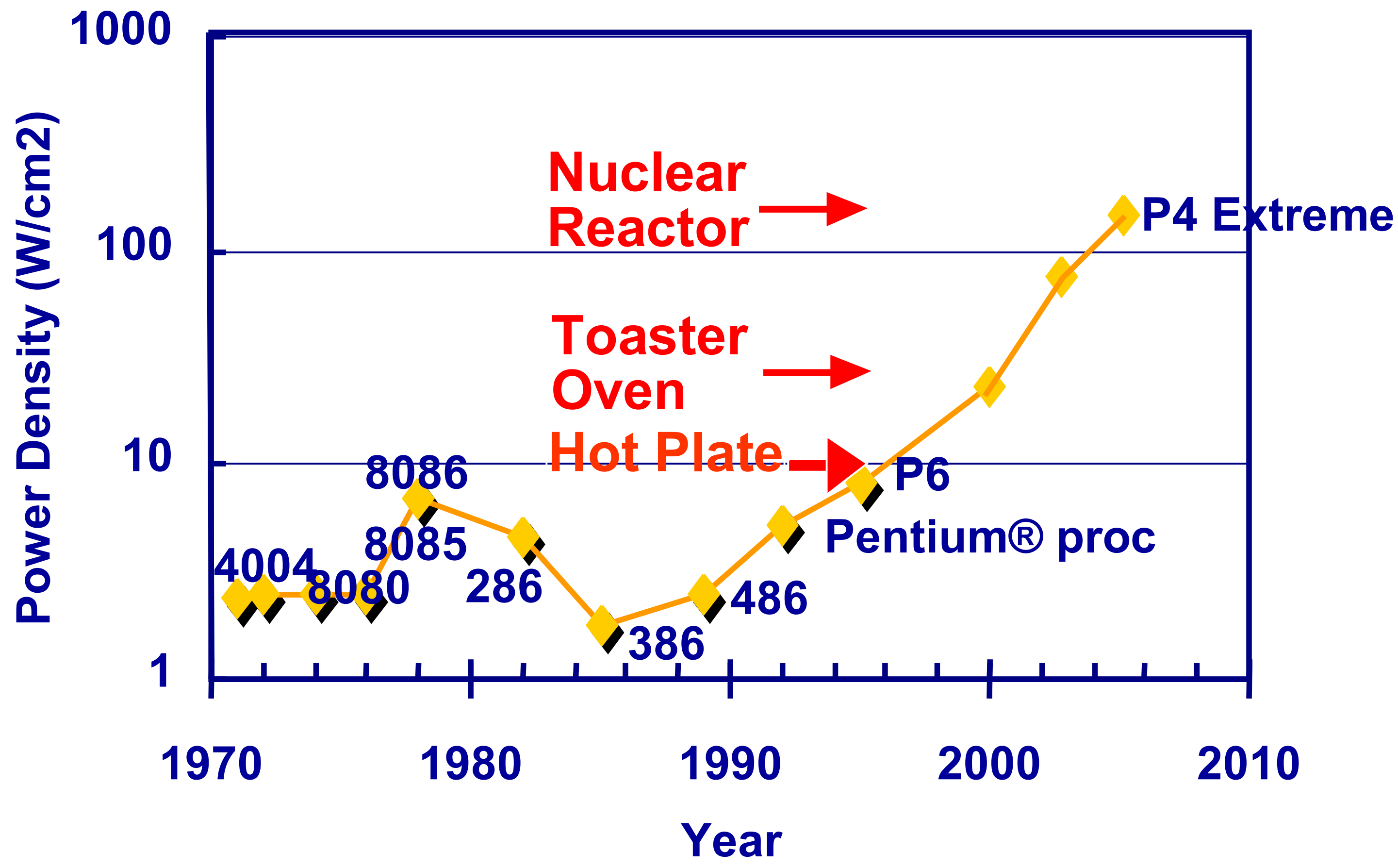
Courtesy, Intel

Power Dissipation



Courtesy, Intel

Power density



Courtesy, Intel

Challenges in Digital Design

∝ DSM

“Microscopic Problems”

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

?

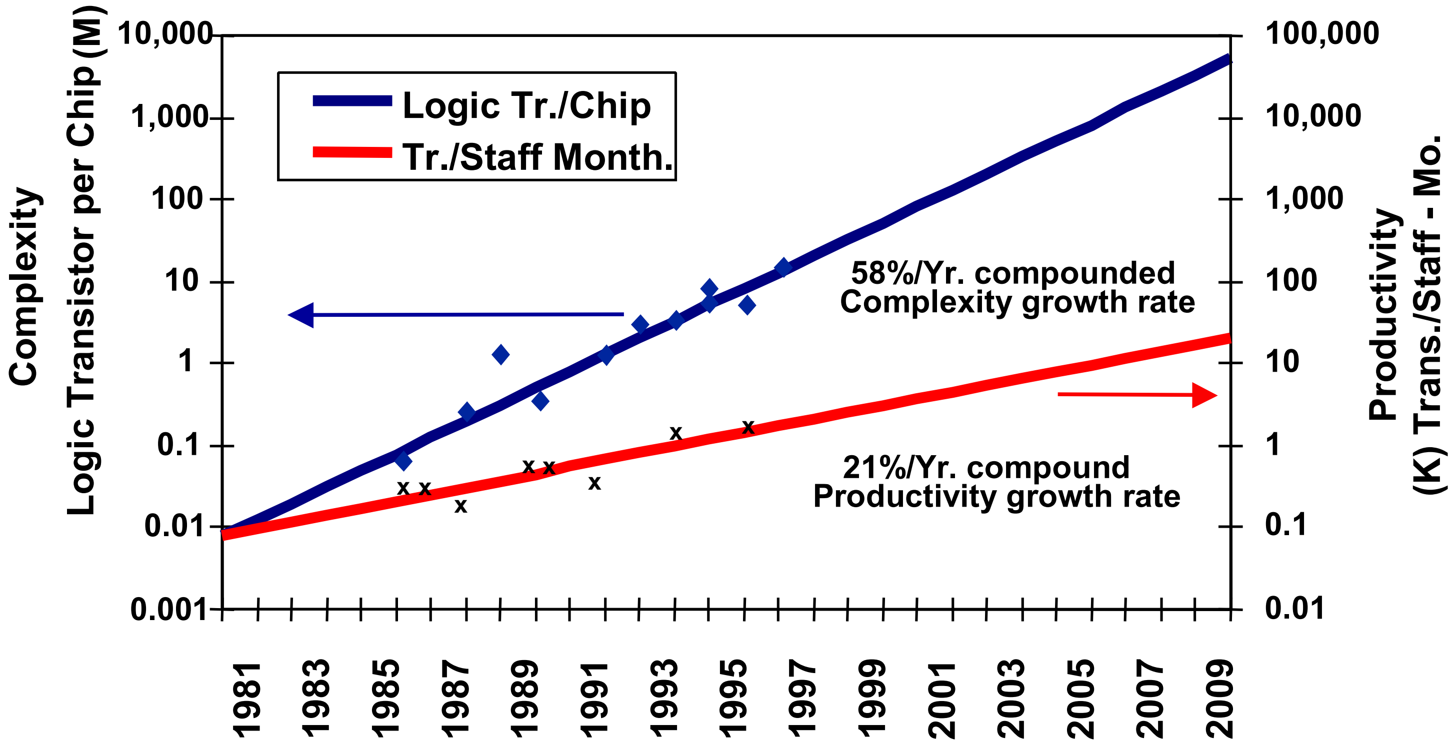
∝ 1/DSM

“Macroscopic Issues”

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

…and There’s a Lot of Them!

Productivity Trends



Source: Sematech

Complexity outpaces design productivity

Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
  - Physical design constraints more and more difficult to surmount
  - Diminishing Returns for Design Dollars

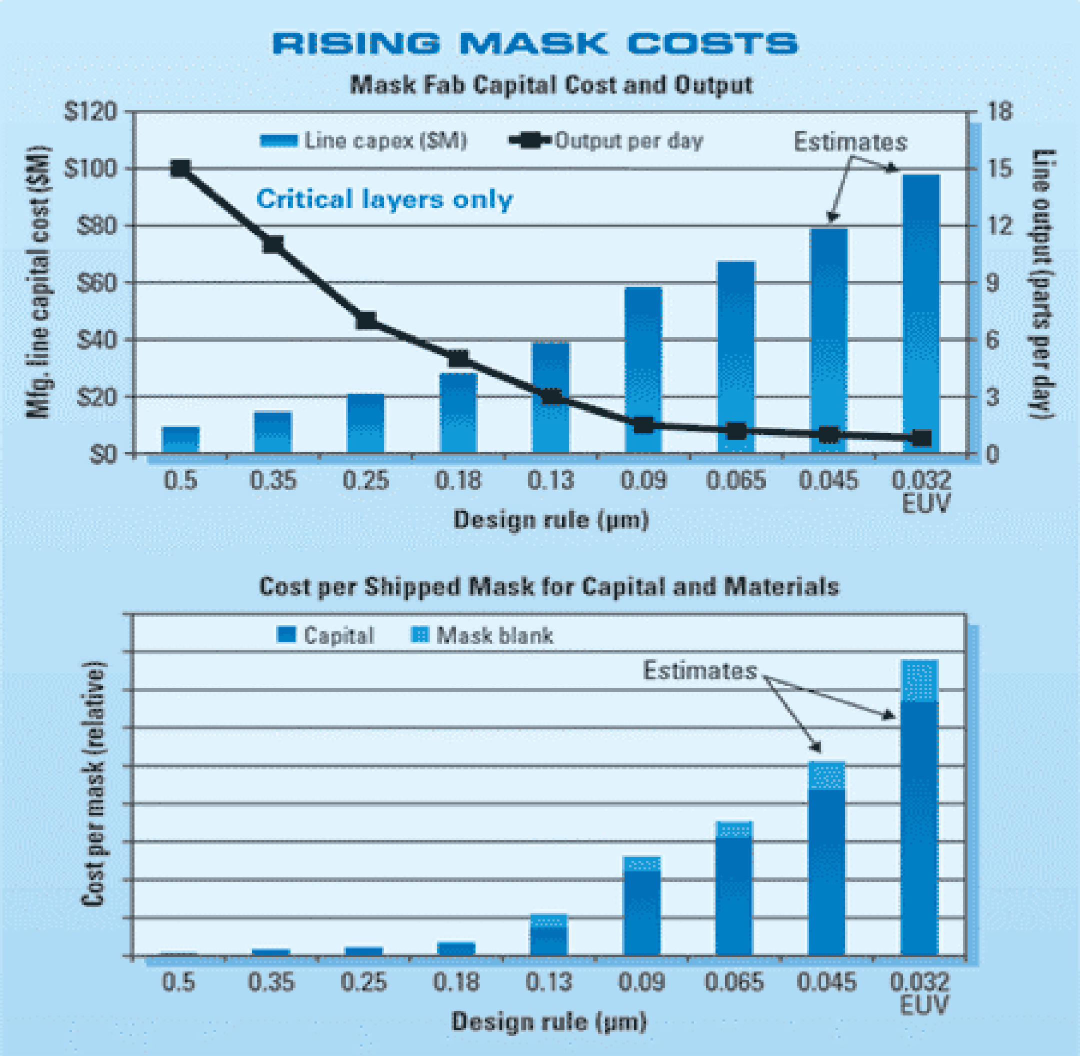
Design Metrics

- ☐ How to evaluate performance of a circuit (gate, block, subsystem)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

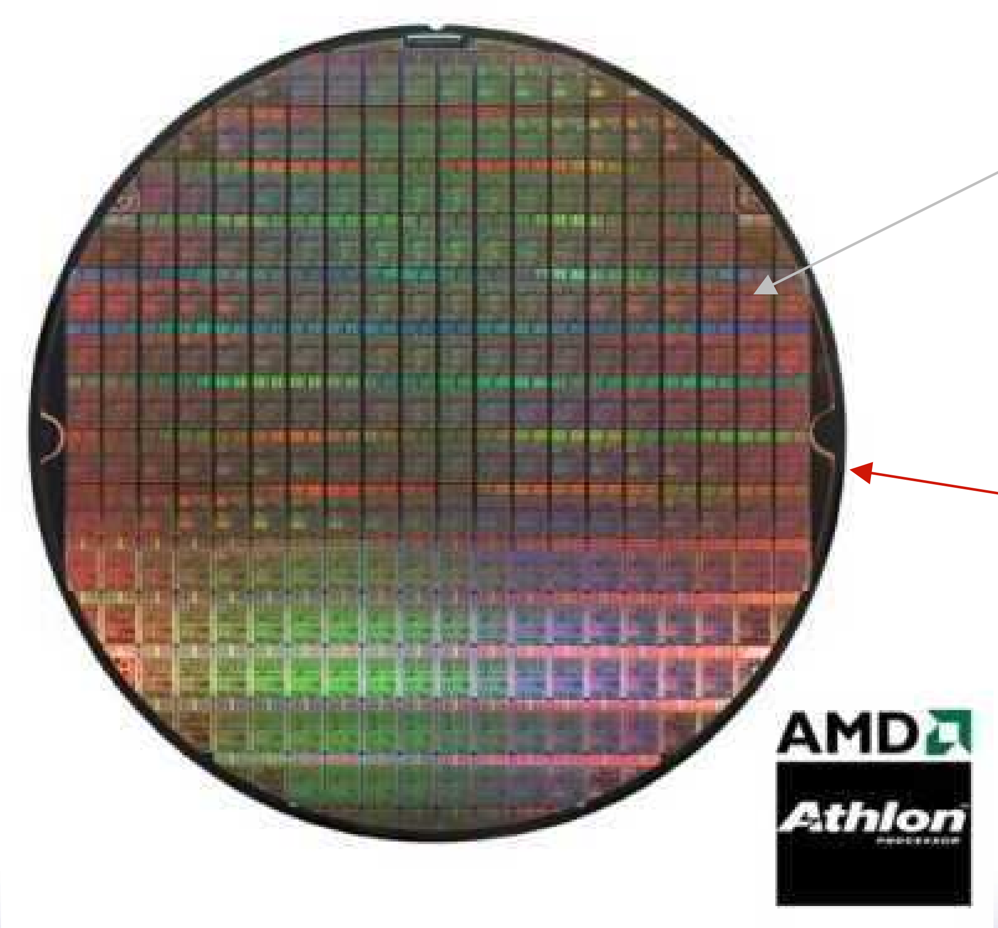
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort
  - mask generation
  - validation and debug
- Recurrent costs
  - silicon processing (cheap/unit!)
  - packaging, test (not cheap!!)

NRE Cost is Increasing



Die Cost



Single die

Wafer

12″ wafer (300mm)

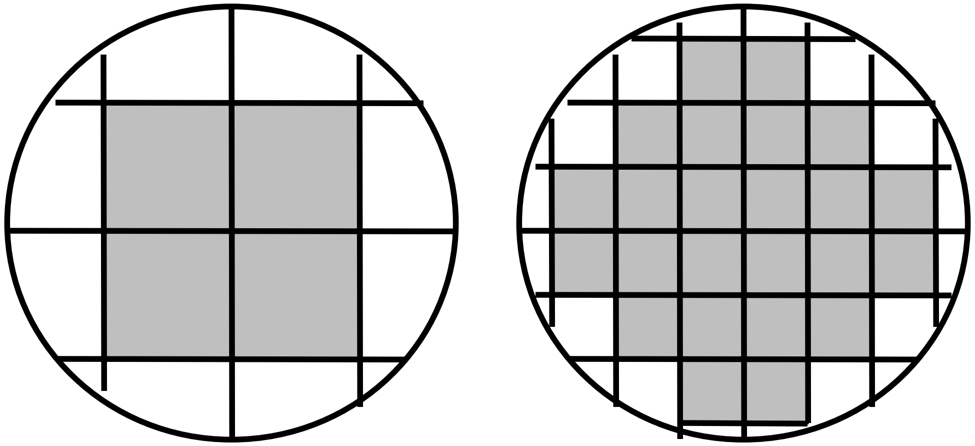
From http://www.amd.com

Yield

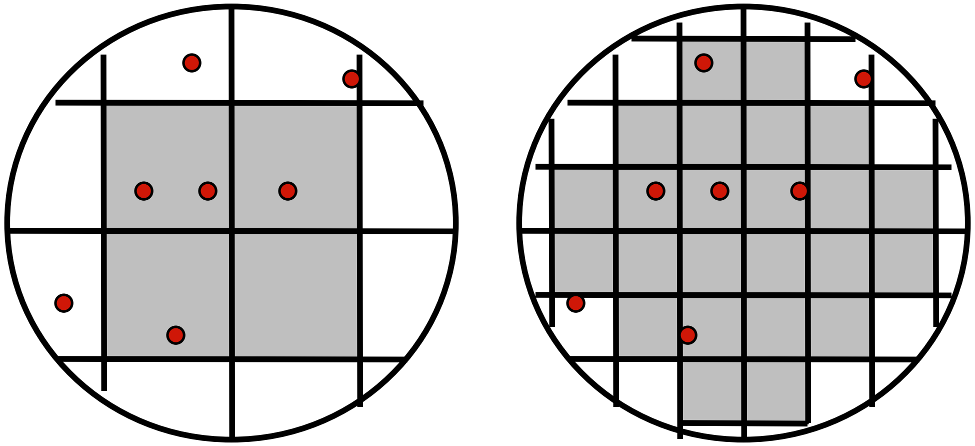
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times \left(\text{wafer diameter/2}\right)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects

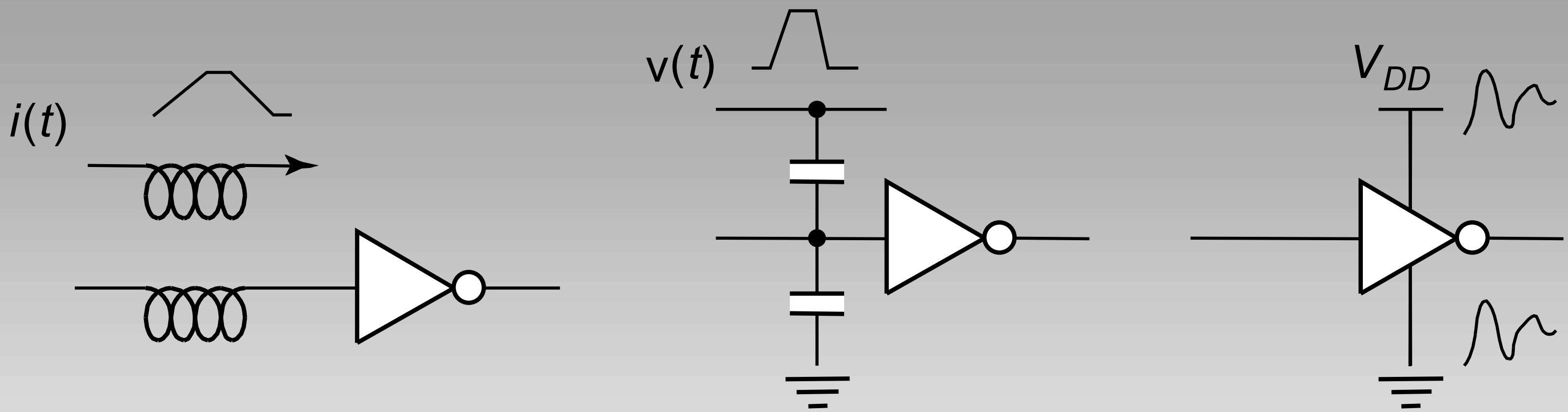


$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

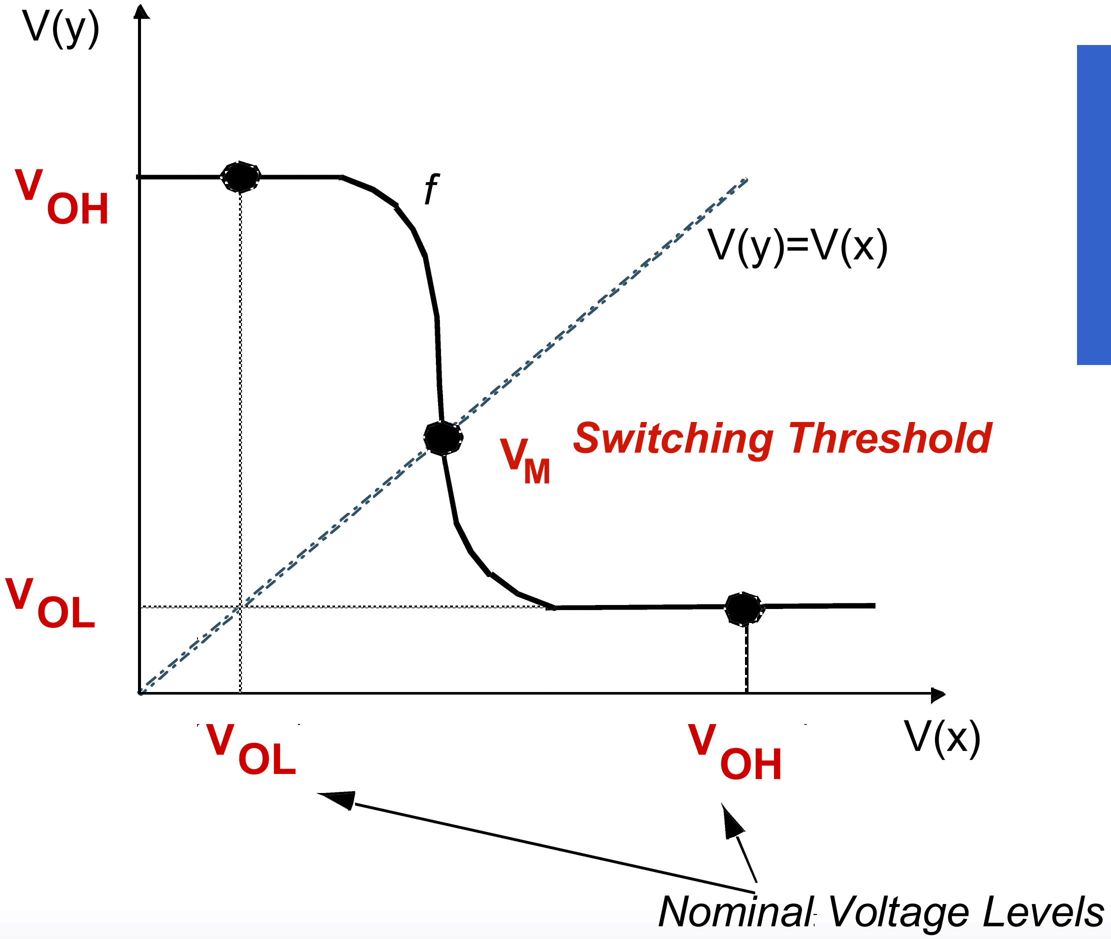
$$\text{die cost} = f\,(\text{die area})^4$$

Reliability—
Noise in Digital Integrated Circuits



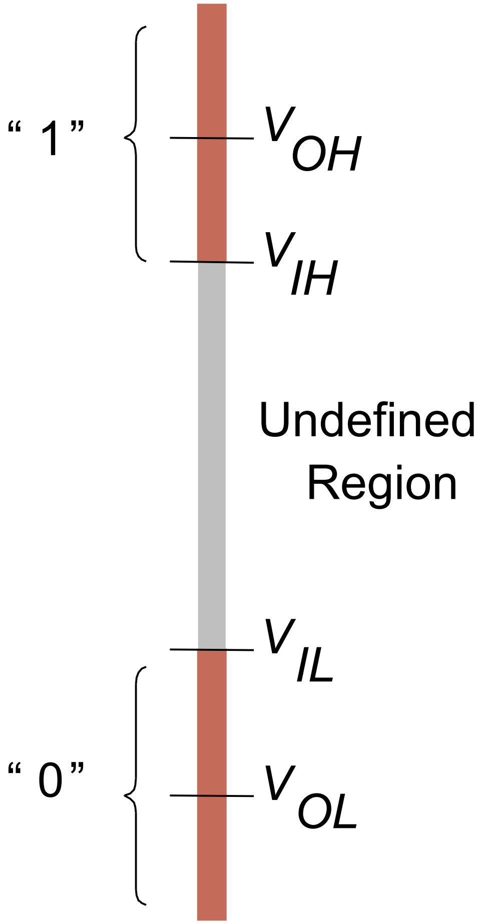
Inductive coupling **Capacitive coupling** **Power and ground noise**

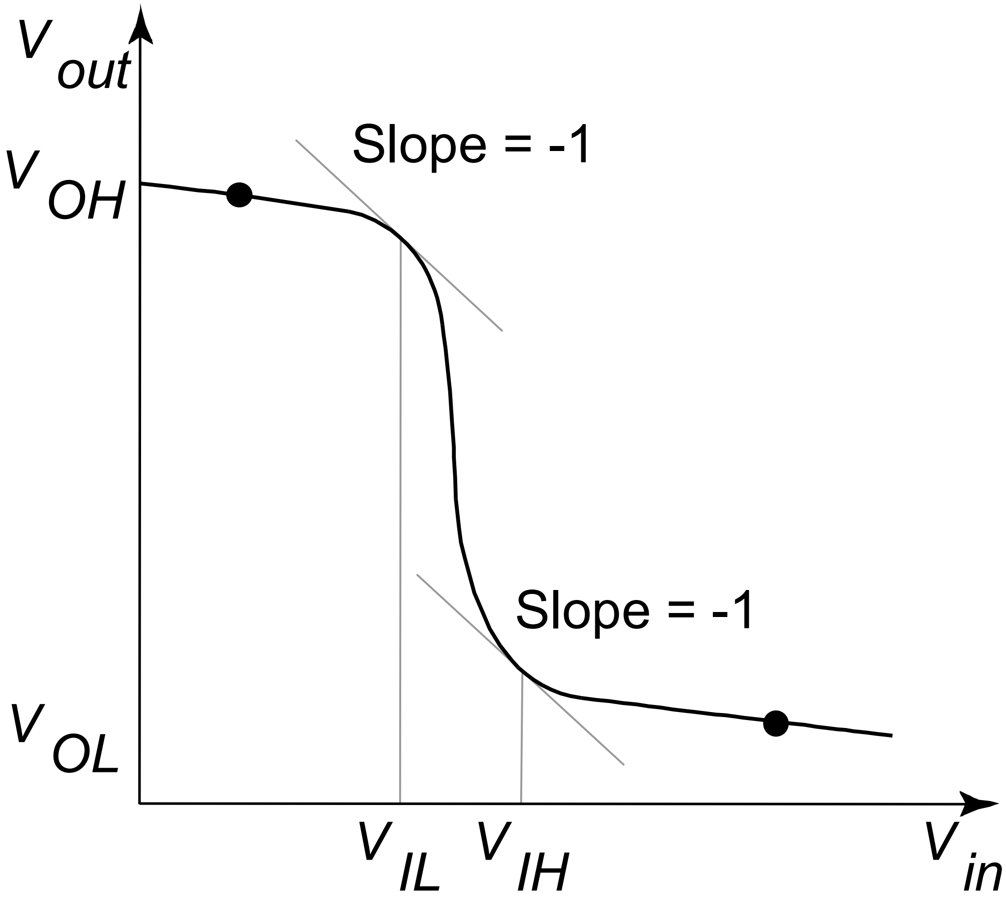
DC Operation
Voltage Transfer Characteristic



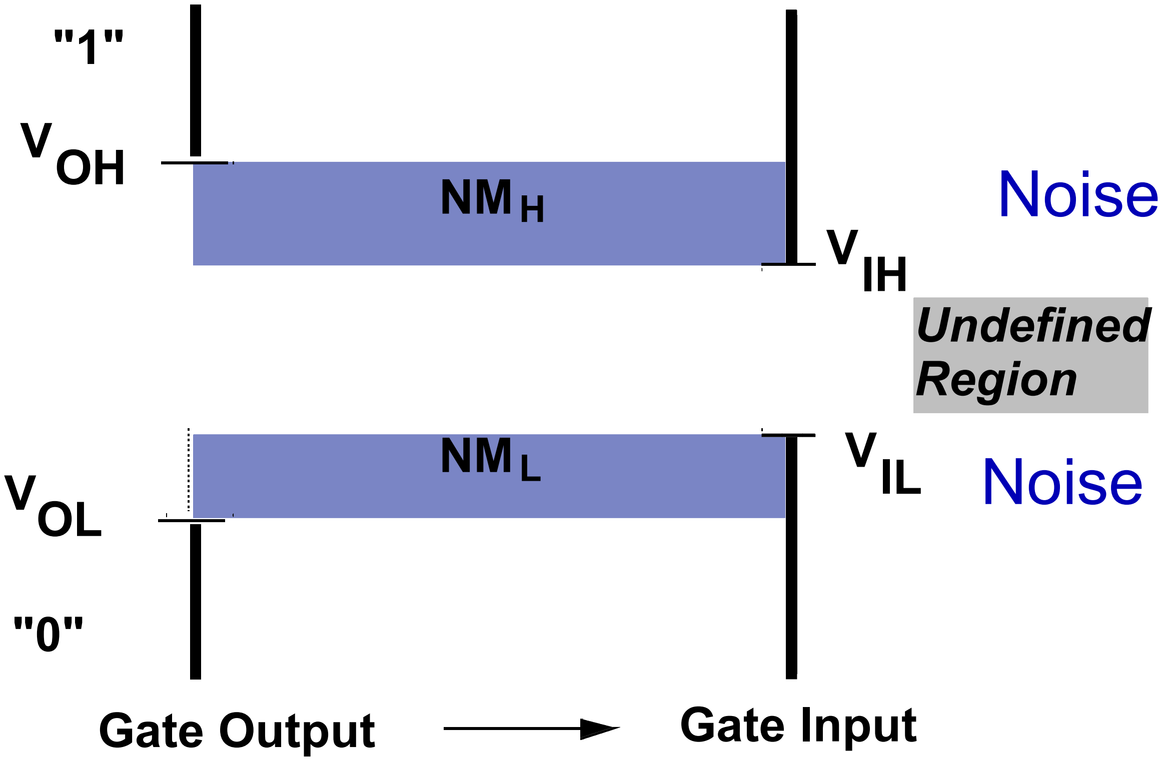
VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

Mapping between analog and digital signals





Definition of Noise Margins



Noise margin high

Noise margin low

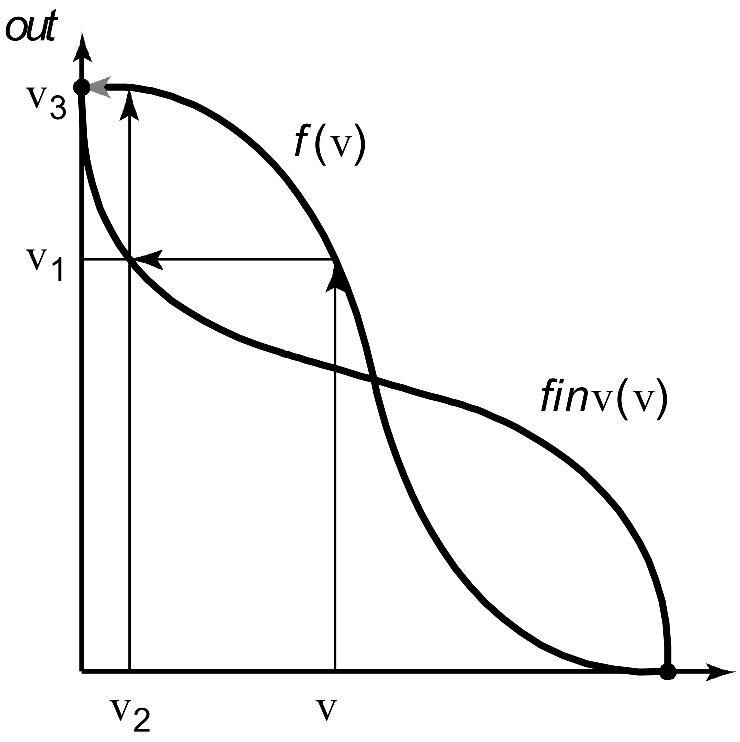
Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources

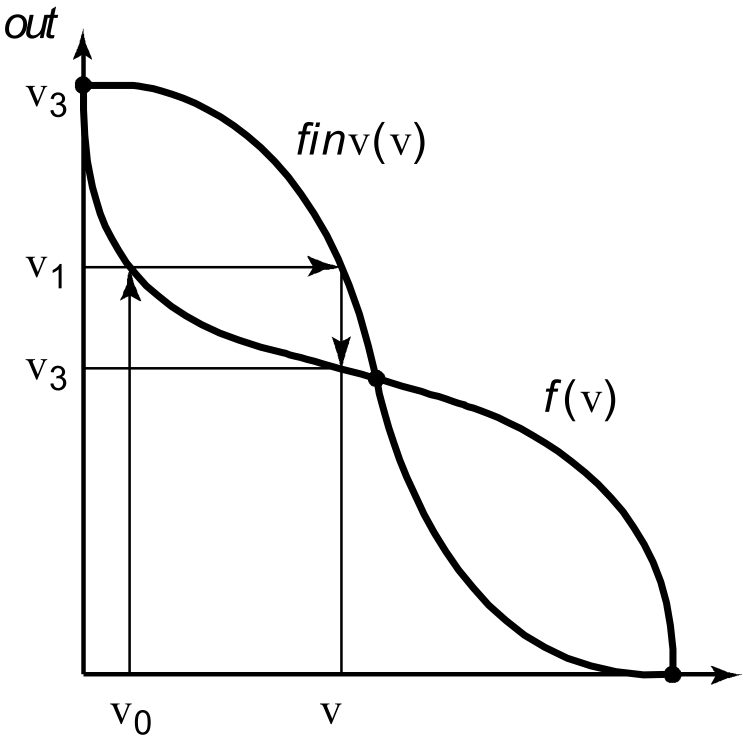
Key Reliability Properties

- Absolute noise margin values are deceptive
    - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

Signal Regeneration

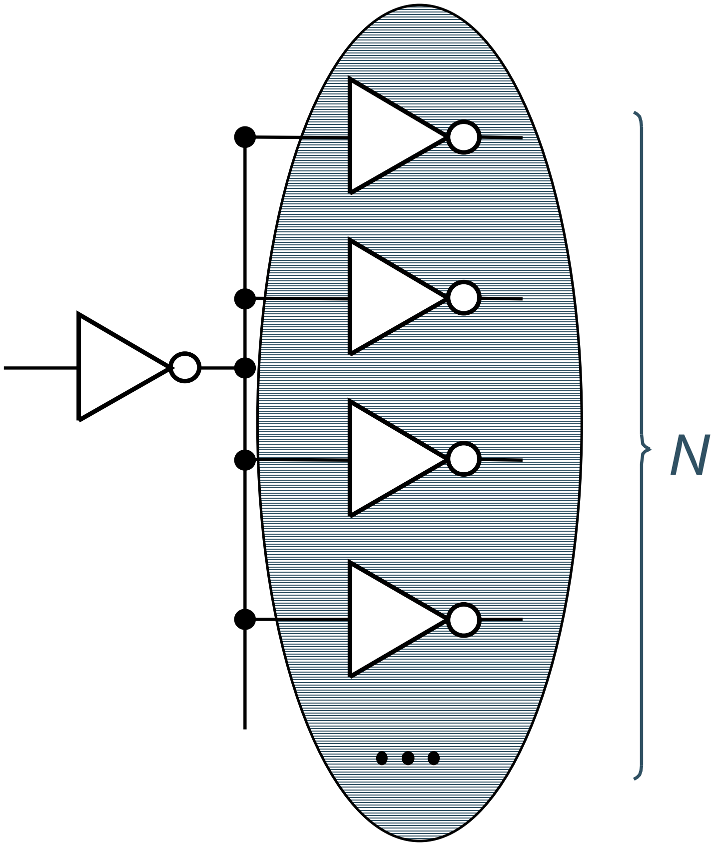


Regenerative

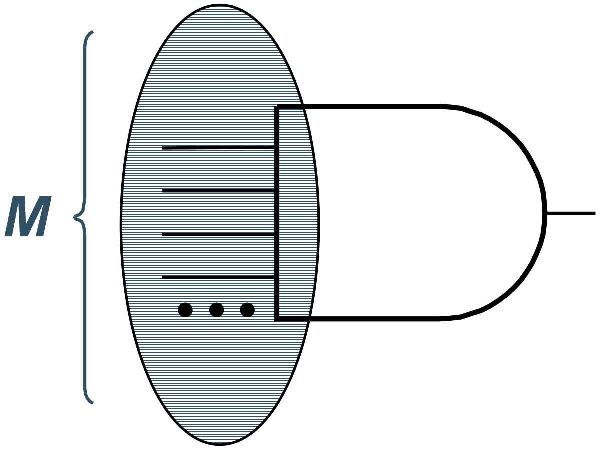


Non-Regenerative

Fan-in and Fan-out

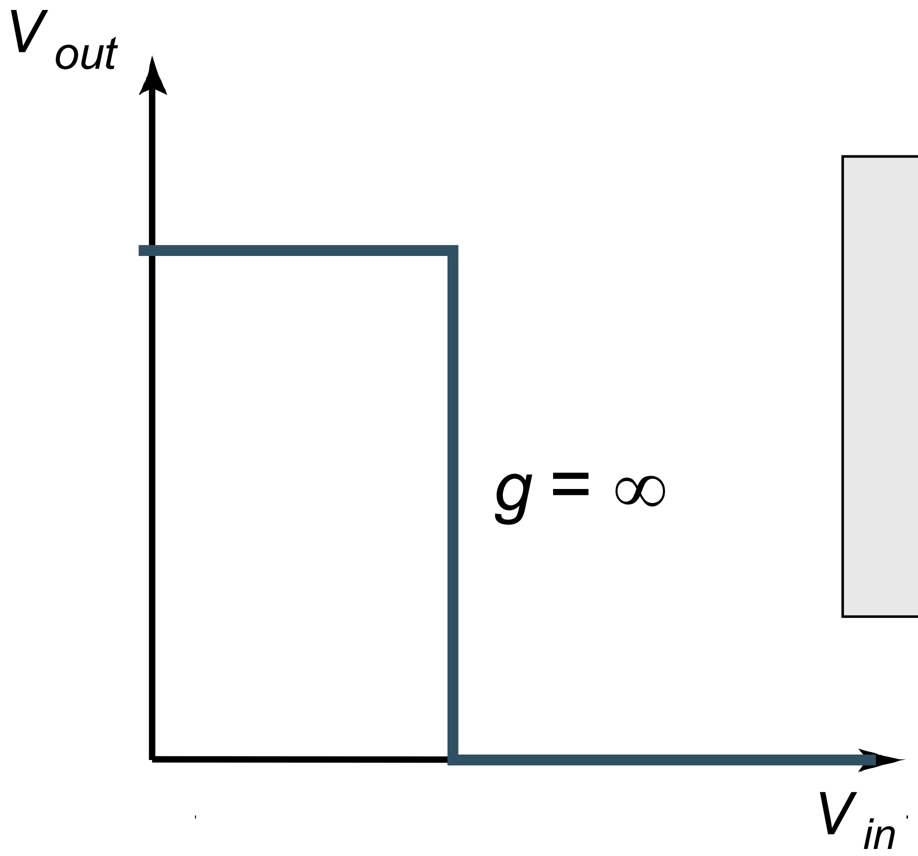


Fan-out *N*



Fan-in *M*

The Ideal Gate



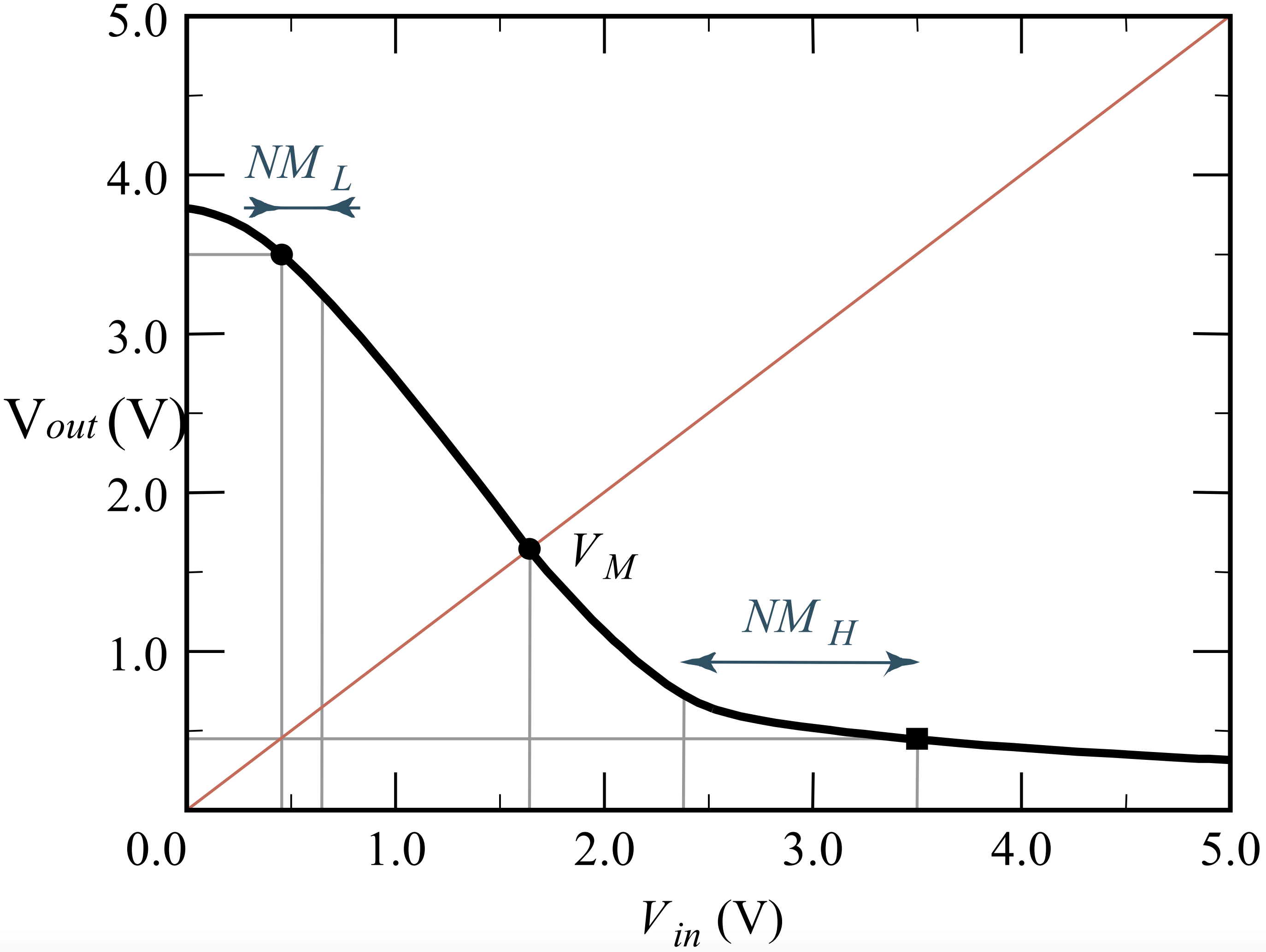
$R_i = \infty$

$R_o = 0$

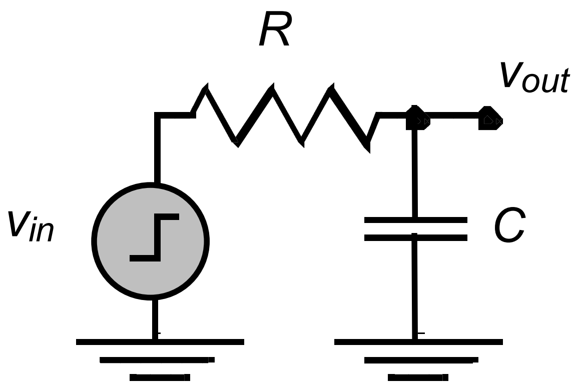
$\text{Fanout} = \infty$

$NM_H = NM_L = V_{DD}/2$

An NMOS Inverter



A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

$t_p = \ln(2)\, \tau = 0.69\, RC$

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}\left(t\right)dt$$

Energy and Energy-Delay

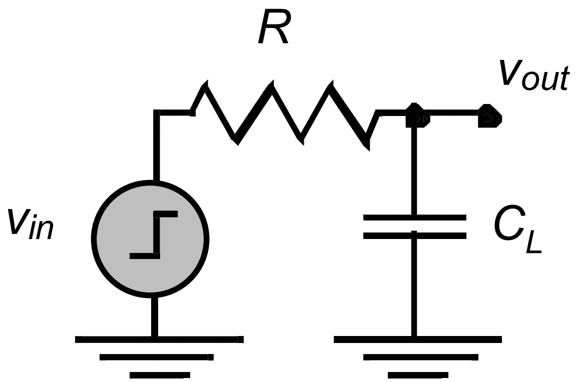
Power-Delay Product (PDP) =

E = Energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$

A First-Order RC Network



$$E_{0\rightarrow 1} = \int_0^T P(t)dt = V_{dd}\int_0^T i(t)dt = V_{dd}\int_0^{V_{dd}} C_L dV_{out} = C_L V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out}(t)i(t)dt = \int_0^{V_{dd}} V_{out} C_L dV_{out} = \frac{1}{2} C_L V_{dd}^2$$

Summary

- ☐ Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- ☐ Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this book
- ☐ Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation

Lecture Problems 1

1. If 4” wafers cost $400, 6” cost $800 and 10” cost $1300 estimate the cost of a 5x5mm die in each case, given a point defect rate 0.3/sq cm. How does that compare to a 7x7mm and 10x10mm die?
2. Go to the ITRS website: http://www.itrs.net and download the 2004 overview update document. Note the update changes and summarize the few significant issues (e.g. chip power dissipation)
3. Analog circuits can easily be fabricated in finer scale technologies – yet lag by orders of magnitude in size from digital designs. Why is this so? (Hint: consider the effects of composing two working analog sub-circuits into a larger circuit.)
4. Please explain the difference between energy dissipation in a gate model and that stored in a capacitor. Where does the ½ come from?
5. FPGA (field programmable Logic arrays) are growing into many designs replacing ASICS. Explain why such designs can compete given a typical 30-50x performance reduction compared to native custom circuits in the same technology.
6. An alternative to full custom ASICS are gate array devices– where the lower level masks are fixed and the upper level metal masks are not. Thus NRE is substantially lower. Compare to FPGA solutions in cost and performance. (Feel free to peruse marketing literature..)