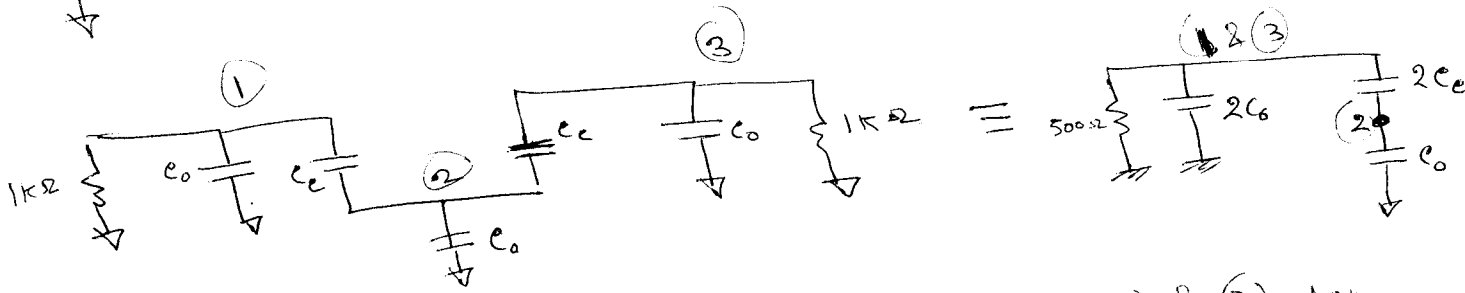
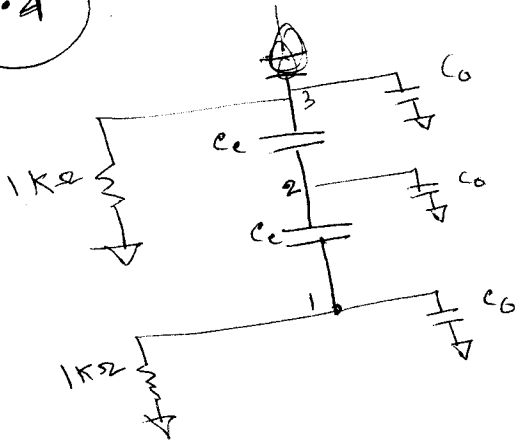


6.4

H.W - 8 solutions



$C_{eq} = 2C_0 + \frac{2C_c C_0}{2C_c + C_0}$ [\because voltages at ① & ③ same]

$\tau = R C_{eq}$

$V_{1,2,3} = e^{-\frac{t}{\tau}}$

voltage lost in bit 2 line.

$V_{lost} = \frac{2C_0}{2C_c + C_0} \Delta V_{1,3} \rightarrow +1V$

$V_2 = 1 - V_{lost}$

$V_{bit2}(t) = V_2 + V_{lost} e^{-\frac{t}{\tau}}$

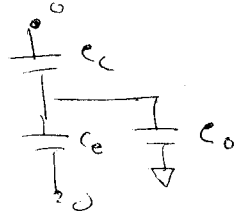
$$\tau_{pv} \gg \tau_{pd}$$

① & ③ reached ∞

$$C_{eff} = 2C_c + C_o$$

$$\tau' = R C_{eff}$$

$$V_2 = 1 + \left(c_1 e^{-\frac{t}{\tau'}} + c_2 e^{-\frac{t}{\tau}} \right)$$



$$6.7 \quad \Delta I = \frac{\Delta V}{R} \times 128 = \frac{3.3}{50} \times 128 =$$

$$L \frac{\Delta I}{\Delta t} \leq V = 300 \text{ mV}$$

$$L < 0.355 \text{ nH}$$

to reduce inductance use parallel connection of inductance by using multiple pins

$$\frac{L}{n} \leq 0.353 \text{ nH} \Rightarrow n \geq 190.8$$

$$n \approx 191$$

$$\Delta t = 3 \text{ ns}$$

$$n \geq \frac{L}{V} \frac{\Delta I}{\Delta t}$$

$$n \approx 97$$

9-2, 3, 4, 5, 7, 8
3 3 3 3 3 3

9-2)

A	000
B	001
C	010
D	011
E	100
F	101
G	110
X	111

⇒ Let X carry event information
That is, every time the X bit is switched
a new event occurs

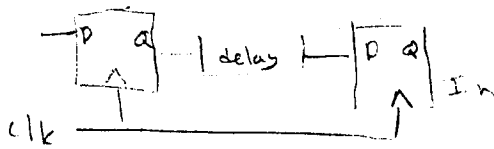
⇒ In addition to this the X-bit could be sent
before a signal to indicate that the letter
occurred at the same time as the letter before

Both of these encoding schemes have drawbacks
In the first case X acts as a sort of clock,
and events can only be determined on the time
scale that is the period of X
In the second case one could use real-time switching,
but events could not take place on a shorter
time-scale than the 111 signal could be established

⇒ minimum clock period

$$T_{min} = T_{C-Q} + T_{logic} + T_{su} + \delta$$

↑ clock delay ↑ logic delay ↑ setup time ↑ skew



In addition the skew has to be smaller than a certain value

$$\delta < T_{C-Q} + T_{logic} - T_{hold}$$

This ensures that the 2nd FF catches the correct value

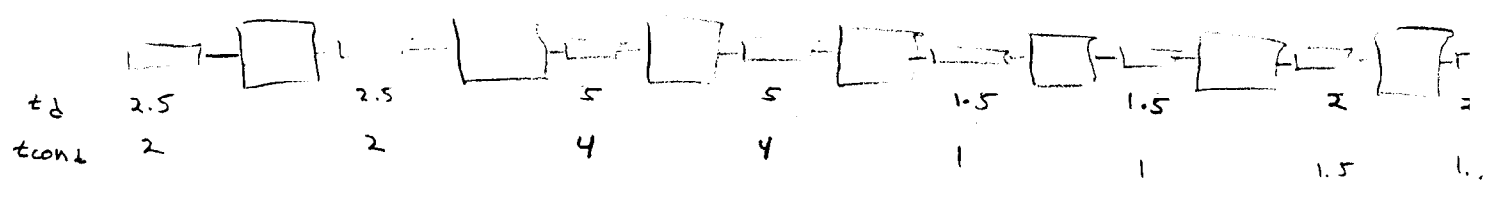
To implement a skew tolerant design the t_{wh} time must be bigger than the skew. This is assuming that the delay is unknown. In addition, the minimum low period,

$$t_{wl} = T_{C-Q} + T_{logic} + T_{su} + \delta$$

so, the minimum total period is increased by the skew

Note: This analysis does not take into account jitter, which can be added to T_{min} , and the maximum δ function

q-4



~~tdd~~

neglect these

$$t_{cy} \geq t_{uB} + t_{u\phi_{it1}} + t_a + t_{rB}$$

$$t_{uB} = t_{uAB} + t_{uA1}$$

$$\text{where } t_{uA1} \approx \frac{t_w}{2}$$

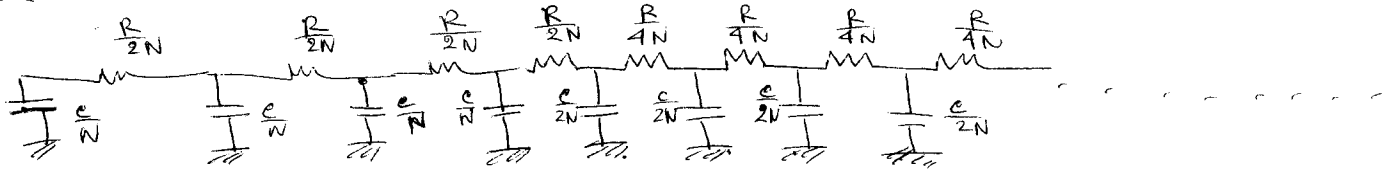
⇒ If assume 50% duty cycle

$$t_w = \frac{1.2 \text{ ns}}{2} = 0.6 \text{ ns}$$

$$\text{so, } t_{cy} = 1.2 \text{ ns} + \frac{0.6 \text{ ns}}{2}$$

$$t_{cy} = 1.5 \text{ ns}$$

a)



$$\tau = \frac{1}{N^2} \left[\frac{Rc}{2} + Rc + \frac{3}{2} Rc + Rc + \frac{9}{4} Rc + \frac{5}{4} Rc + \frac{11}{8} Rc \dots \right]$$

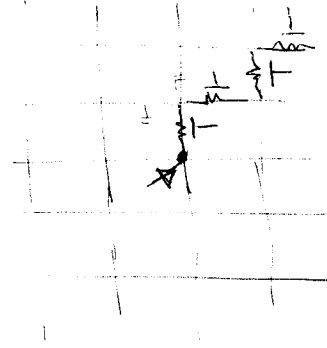
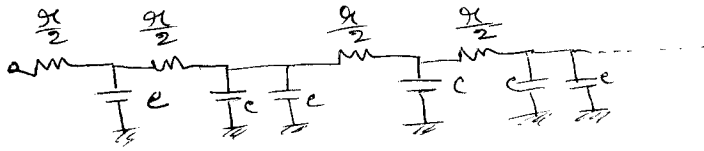
$$\approx \frac{Rc}{N^2} 7.75$$

$$\left[\begin{array}{l} c = 0.28 \text{ pF} \times L \\ R = 250 \times L \end{array} \right]$$

b) $C_{total} = 4^8 \times 7 + \frac{3}{2} L \sqrt{N} \times c$

Power dissipated = $C_{total} V_{DD}^2 f$

8)



However this is a very approximate model as all capacitances ~~are~~ are assumed to be equivalent.

$$\tau = \frac{r}{2} c + 2rc + c + \frac{3r}{2} + 2c \times 2r + \dots$$

where $r = \frac{r l}{N}$

$$c = \frac{c l}{N}$$

N can be found by putting $\tau_r < 200ps$.

b) The resistance of wires near the centre should be made less than those far from centre, so we should use thicker wires near centre & thinner wires far from centre.