

6.1

① This takes into account voltage drops across the chip with respect to  $V_{IR}$  &  $L \frac{di}{dt}$  in the power distribution network.

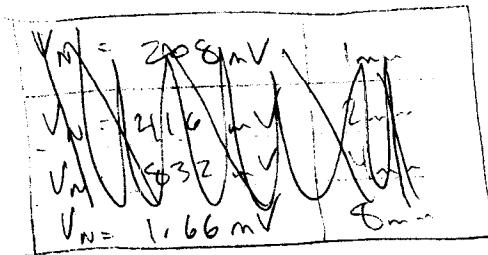
②  $C_L = 100 \text{ fF}$ ,  $10^4 \text{ gates}/\text{mm}^2 = 1 \text{ nF}/\text{mm}^2$   
 $\frac{1}{3} C_L$  supply, thus  $333 \text{ pF}/\text{mm}^2$

$$I_P = \frac{C_L V_P}{t_{ck}} = \frac{(333 \text{ pF}/\text{mm}^2)(2.5 \text{ V})}{5 \text{ ns}} = 167 \text{ nA}$$

$$L \approx 4 \frac{I_{peak}}{I_{avg}} = 4 \Rightarrow I_{avg} = 41.6 \text{ mA}$$

~~$V_N = (2.5 \text{ V})(41.6 \text{ mA})$~~   
 ~~$V_N = 104 \text{ mV}$~~

$$V_N = I_{avg} R + L \frac{di}{dt}$$



③ There is an equal distance when transiting perpendicular thus the duration is the same

Assume single layout



$$L_P \leq \frac{K_P \cdot 211}{10^{-3} I_{avg}} \Rightarrow L_P \leq \frac{(0.25)(2)(12 \text{ mm})}{(10^{-3})(0.165)}$$

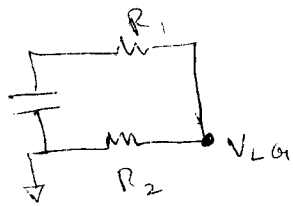
$L_P \leq 3.07 \text{ mm}$

6.2

Initially when switch at upper position,

$$V_{LP} = 3.3, \quad V_{Lor} = 0$$

Now when it comes to lower position



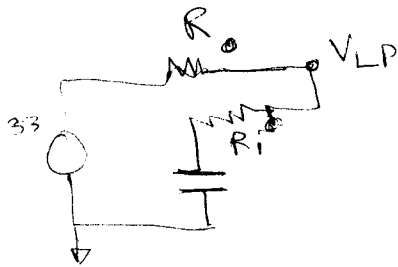
$$\text{Let } R = R_1 + R_2$$

$$I(t) = \frac{V_0}{R} e^{-\frac{t}{RC}}$$

$$V_{Lor} = R_2 I(t)$$

$V_{Lor}$  rises above 0, so source voltage of gates no longer at 0, so the threshold voltage of the ~~gate~~ transistors changes.

When switch is at upper position

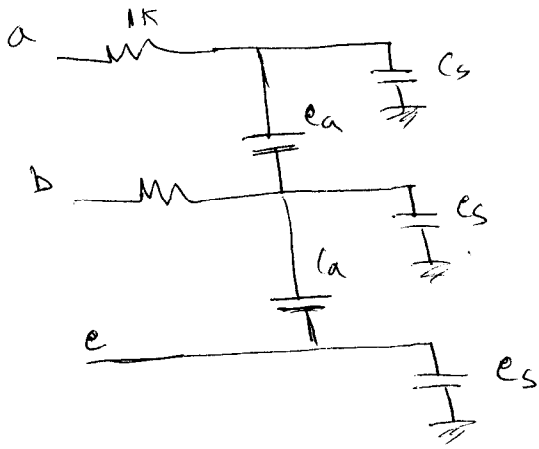


The 3.3V supply charges the capacitor.

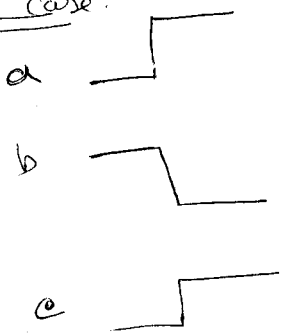
$$V_{LP} = 3.3 - R_0 I(t)$$

Thus the  $V_{LP}$  changes as a function of time.

6.2



Worst case.

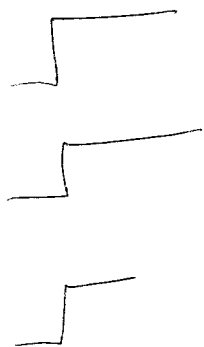


due to Miller effect

$$e_{Total 1} = e_s + (2C_a + 2C_b) \text{ (line a)} + 2C_e \text{ (line e)}$$

$$\tau = R C_{Total}$$

best case



$$e_{Total 2} = e_s$$

$$\tau = R e_{total 2}$$