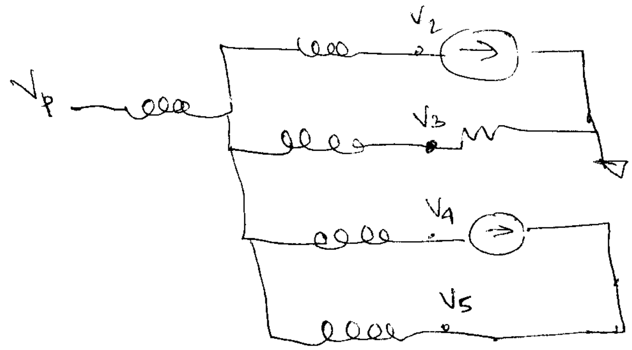
HW-6 solution

5.1)



$V_2 = 2.5 - 10\,nH \times 2 \times \frac{1}{10\,ns} = 0.5V$

I_R (current through resistor) $= \frac{2.5}{10} = 0.25$ initially

$= \frac{1.5}{10} = 0.15$ after I_1 is switched.

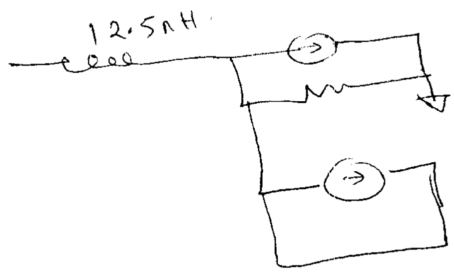
$V_3 = 1.5 - 10 \times \frac{0.1}{10} = 1.4V$

$V_4 = 1.5 - 10 \times \frac{1}{10} = 0.5$

$V_5 = 1.5 + 10 \times \frac{1}{10} = 2.5$

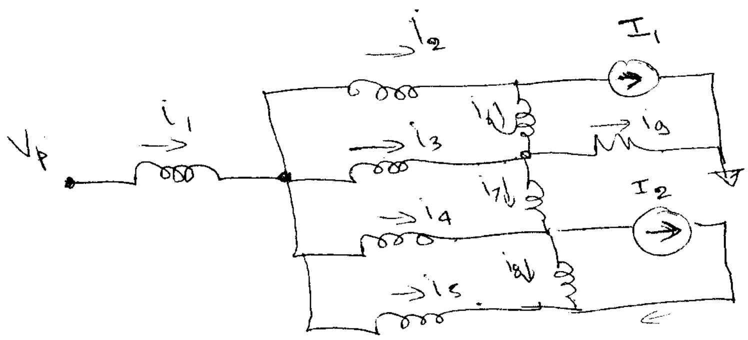
When they are connected

$\frac{1}{L} = \frac{1}{10} + \frac{1}{10} + \frac{1}{10} + \frac{1}{10} \Rightarrow L = 2.5\,nH.$



$V_2 = V_3 = 2.5 - 12.5 \times \frac{1}{10} = 1.25.$

$V_4 = V_5 = V_2$



$$i_1 = i_2 + i_3 + i_4 + i_5$$

$$i_2 = i_6 + I_1$$

$$i_3 + i_6 = i_9 + i_7$$

$$i_4 + i_7 = I_2 + i_8$$

$$i_5 + i_8 + I_2 = 0$$

$L = 60\,nH$
$L' = 5\,nH$

$$V_p - L\frac{di_1}{dt} - L\frac{di_3}{dt} = i_9 R$$

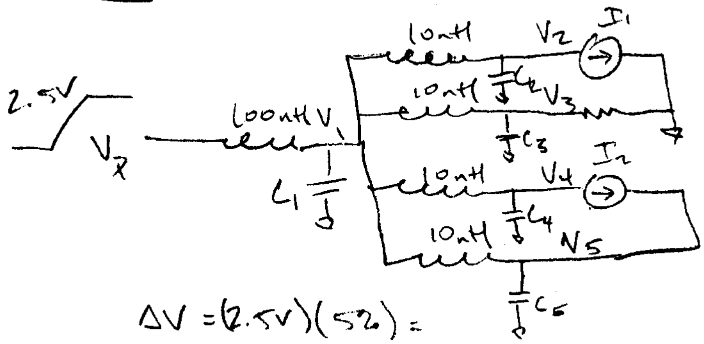
$$V_p - L\frac{di_1}{dt} - L\frac{di_4}{dt} - L'\frac{di_8}{dt} = V_p - L\frac{di_1}{dt} - L\frac{di_5}{dt}$$

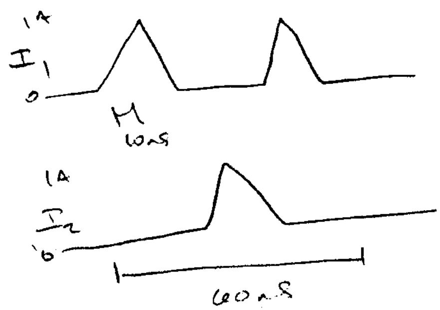
$$V_p - L\frac{di_1}{dt} - L\frac{di_2}{dt} - L'\frac{di_6}{dt} = i_9 R$$

$$V_p - L\frac{di_1}{dt} - L\frac{di_4}{dt} = i_9 R - L'\frac{di_7}{dt}$$

9 equations => 9 unknowns, solve to get currents and voltages at V_2, V_3, V_4, V_5

15.2





$\Delta V = (2.5V)(5\%) =$

$\Delta V = 0.125V$

$$C > L\left(\frac{I_{Avg}}{\Delta V}\right)^2$$

$I_{Avg\,V_1} = (\#\text{ Transfers}) \cdot (\text{Area of triangle}) / \Delta T$

$= 3 \cdot \frac{1}{2} \cdot 20nS \cdot 1A \;/ 60nS$

$I_{Avg_1} = 0.5A$

$$C_{B_1} > 100nH\left(\frac{0.5A}{0.125V}\right)^2$$

$\boxed{C_{B_1} = 1.6\mu F}$

$I_{Avg\,V_{2,3}} = 2 \cdot \frac{1}{2} \cdot 20nS \cdot 1A \;/ 60nS = 0.334A$

$I_{Avg}\,V_{3,4} = 1 \cdot \frac{1}{2} \cdot 20nS \cdot 1A \,/ 60nS = 0.167A$

$$C_{B_{2,3}} > 10nH\left(\frac{0.334A}{0.125V}\right)^2$$

$\boxed{C_{B_{2,3}} = 71.1nF}$

$$C_{B_{4,5}} > 10nH\left(\frac{0.167A}{0.125V}\right)^2$$

$\boxed{C_{B_{4,5}} = 17.8nF}$

[redacted]

Key

5.11

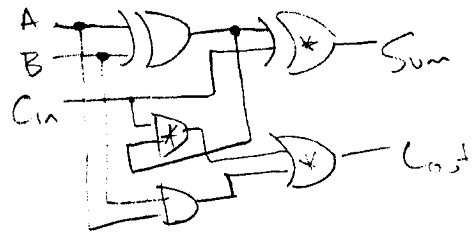
(A) Assume Gate with parameters

$V = 2.5V$

$I_{avg} = 13 \mu A$

$I_{peak} = 1.4 mA$

$\tau = 200 pS$



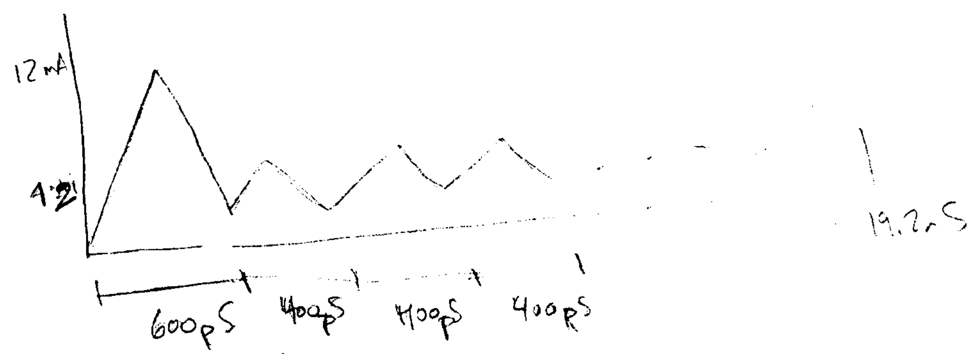
$\tau_p = C_{out\ delay} = 3$ gate delays $= 600 pS$

Worst case delay

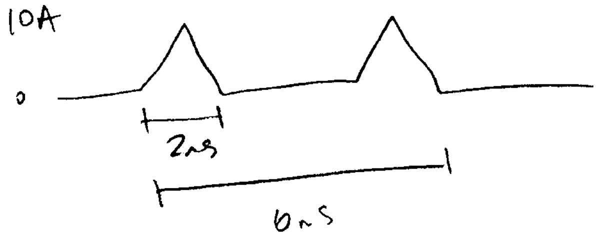
$C_{out\ delay}$ (# cells) $\Rightarrow (600pS)(32) = 19.2 nS$

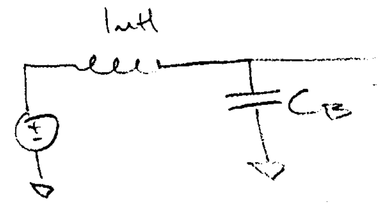
$I_{C_{out}} = (3 \text{ gates*})(1.4 mA) = 4.2 mA$

$I_{peak\ cell} = (5 \text{ gates})(1.4 mA) = 12 mA$



5.12





Assume 2.5V

$\Delta V = (2.5V)(5\%) = 0.125V$

$f = \frac{1}{T} = 167MHz$

$$I_{Avg} = \frac{\frac{1}{2} \cdot 2ns \cdot 10A}{6ns} = 1.67\,A$$

$$C_B > \frac{I_{avg}}{\Delta V}\left(k_i t_{ck} + \frac{L \cdot I_{avg}}{\Delta V}\right) \qquad k_i = \frac{1}{4} \text{ for triangle wave}$$

$$C_B = \frac{1.67A}{0.125V}\left(0.25 \cdot 6ns + \frac{1\mu H \cdot 1.67A}{0.125V}\right) = 179\mu F$$

SMT

$$C > \frac{k_i \cdot I_{avg}\, t_{ck}}{\Delta V} = \frac{\frac{1}{2} \cdot 1.67 \cdot 6ns}{0.125} = 40\,nF$$

Use 40 - 1nF, 0.1Ω, 1nH SMT at 160MHz

Aluminum Electrolytic

$$C > L\left(\frac{I_{avg}}{\Delta V}\right)^2 = 1\mu H\left(\frac{1.67A}{0.125}\right)^2 = 178\mu F$$

Use 18 - 10μF, 1Ω, 10nH at 160kHz & 16MHz

5.13

15 mm × 15 mm with 1M gates ~ 4444 gates/mm²

100 MHz = 10 ns period

$P = C V \Delta V f$

$= (200\,fF)(2.5)(2.5)(16.7\,MHz)$

$P_{gate} = 20.8\,\mu W$

$P_{chip} = P_{gate} * 1\times10^6$

$\boxed{P_{chip} = 20.8\,W}$

Switches every 30 ns thus two switches for period

$f = \frac{1}{60\,ns} = 16.7\,MHz$

fraction of metal devoted to power bus for one polarity

$V_{IR} = \frac{J_{pk} \cdot r_w \cdot L_p^2}{8 \cdot k_p} \Rightarrow k_p = \frac{J_{pk} \cdot r_w \cdot L_p^2}{8 \cdot V_{IR}}$

$\frac{I_{peak}}{I_{avg}} = 4$

$V_{IR} = 10\% \cdot 2.5V = 250\,mV$

Assume $r_w = 40\,m\Omega/square$ — 1 µm thick alum wire From book pg. 241

$L_p = 15\,mm$

$P = IV$

$I_{gate} = \frac{P_{gate}}{V} = \frac{20.8\,\mu W}{2.5V} = 8.4\,\mu A$

$I_{avg\ gate} = 8.4\,\mu A/gate$

$I_{peak} = 8.4\,\mu A \cdot 4 = 33.6\,\mu A/gate$

$J_{pk} = (4444\,gates/mm^2)(33.6\,\mu A/gate)$

$J_{pk} = 148\,mA/mm^2$

$k_p = \frac{(149\,mA/mm^2)(40\,m\Omega/sq)(15\,mm)^2}{(8)(250\,mV)}$

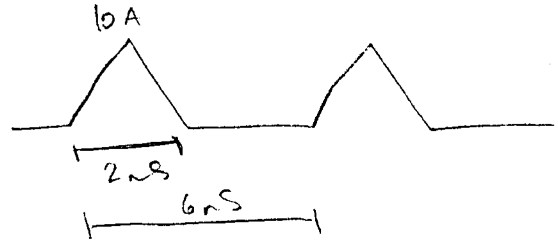
$k_p = 0.668$

thus you need

$\boxed{1.34 \text{ metal layers}}$

5.15

$$C > L\left(\frac{I_{avg}}{\Delta V}\right)^2 = \frac{k_i Q_{ck}}{\Delta V}$$



$$I_{avg} = \frac{Q_{ck}}{\tau} = \frac{\frac{1}{2}\cdot 10A \cdot 2nS}{6nS} = 1.67A$$

$$C_{B_1} > \frac{(0.25)\left(\frac{1}{2}\cdot 10A\cdot 2nS\right)}{0.25V} \Rightarrow 10nF \text{ on chip}$$

$$C_{B_2} > 100nH\left(\frac{1.67A}{0.25}\right)^2 \Rightarrow 4.4nF$$

$$C_{B,total} = 4.4nF + 10nF = \boxed{14.4nF}$$

Much too large to bypass using on chip capacitors

7) a) $i = \frac{2.5}{60\,\Omega} = 40\,mA$.

total current $I = 80 \times 40\,mA = 3.2\,A$

$\left.\frac{dI}{dt}\right)_{worst} = \frac{3.2\,A}{1\,ns} = 3.2\,A/ns$

b) $L\frac{dI}{dt} = 0.25$

$L = \frac{0.25}{3.2} = 0.078\,nH$

no of bumps $= \frac{0.078}{0.5} = 0.156$

c) avg power $= \frac{0.15T \times VI}{T}$

$= 0.15\,VI$

$= 1.2$ watts.