(1)

1) a)

$$f = \overline{a\cdot b + a\cdot c + a\cdot d + b\cdot c + b\cdot d + c\cdot d}$$

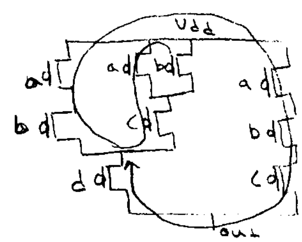
$$\overline{f} = d\cdot(c+b+a) + c\cdot(a+b) + a\cdot b$$

$$f = \overline{a}\cdot\overline{b}\cdot\overline{c} + \overline{a}\cdot\overline{b}\cdot\overline{d} + \overline{a}\cdot\overline{c}\cdot\overline{d} + \overline{b}\cdot\overline{c}\cdot\overline{d}$$

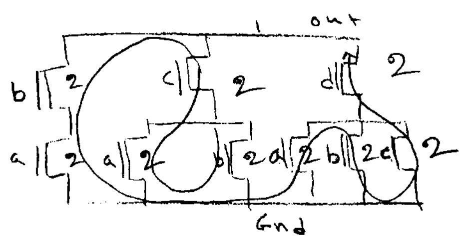
$$= \overline{d}(\overline{a}\cdot\overline{b} + \overline{a}\cdot\overline{c} + \overline{b}\cdot\overline{c}) + \overline{a}\cdot\overline{c}\cdot\overline{b}$$

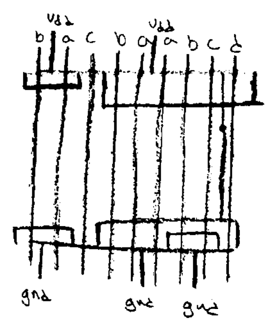
$$= \overline{d}(\overline{c}(\overline{a}+\overline{b}) + \overline{a}\cdot\overline{b}) + \overline{a}\cdot\overline{c}\cdot\overline{b}!$$

PUN:



PDN:

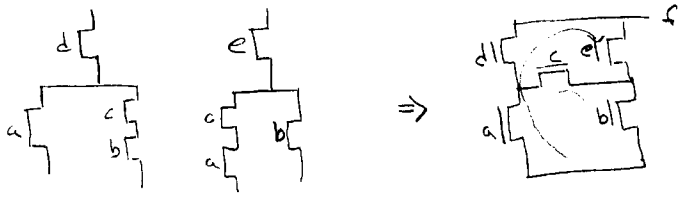




1b) $f = a \cdot d + a \cdot c \cdot e + b \cdot e + d \cdot c \cdot b$

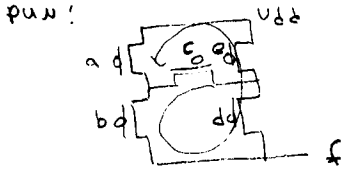
$= d \cdot (a + c \cdot b) + e \cdot (c \cdot a + b)$

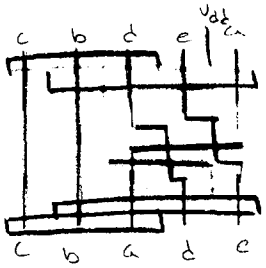
PDN:



Take the dual:

PUN:



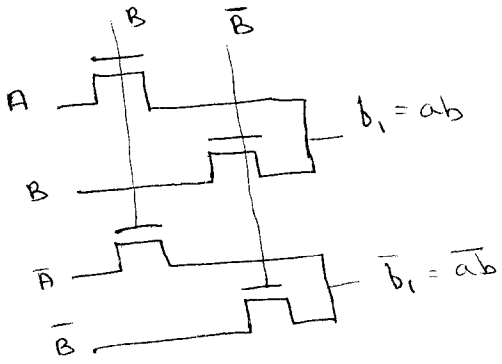


EPL

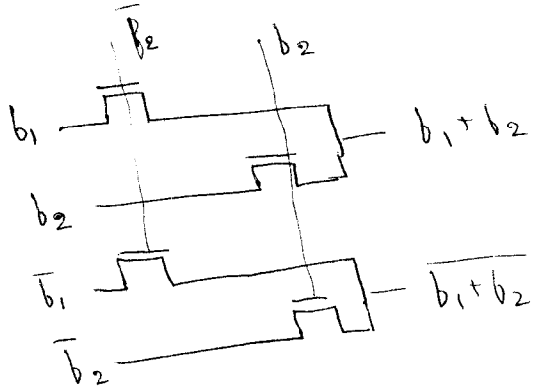
2)

$$f = \overline{ab + ae + ad + bc + bd + ed}$$

$$= \overline{b_1 + b_2 + b_3 + b_4 + b_5 + b_6}$$



→ similarly b_2, b_3, b_4, b_5, b_6 can be found

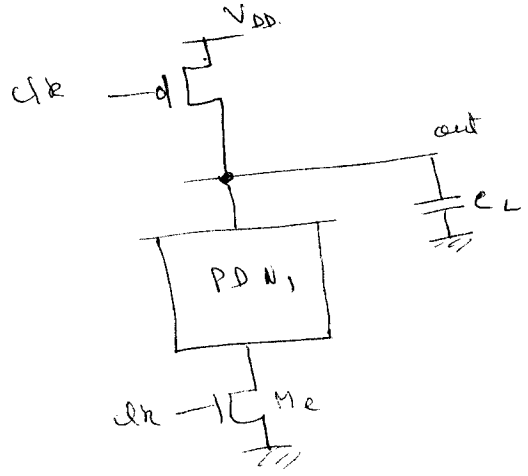


→ proceed in similar manner to find $\overline{b_1 + b_2 + b_3 + b_4 + b_5 + b_6}$

note: no of transistors have not been optimised in this case.

Domino CMOS

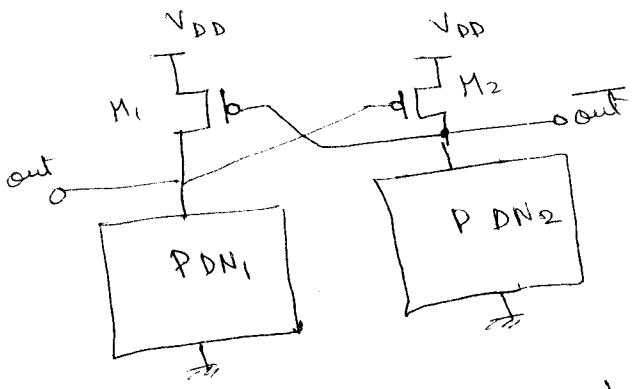
3)



where PDN is the same as in 1a

4

DCSL



PDN_1 is same as as in a

PDN_2 gives inverse logic of PDN_1

3) This is just like two 90 Ω transmission line in parallel

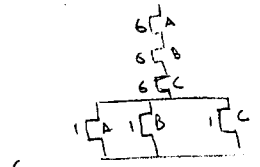
So we can think of effectively a 45 Ω TM line

for 180 nm node, we have $R_{\square} = 8\,K\Omega$

$$\frac{R_{\square}}{S} = 45\,\Omega$$

$$S = \frac{8000}{45} = 177.8$$

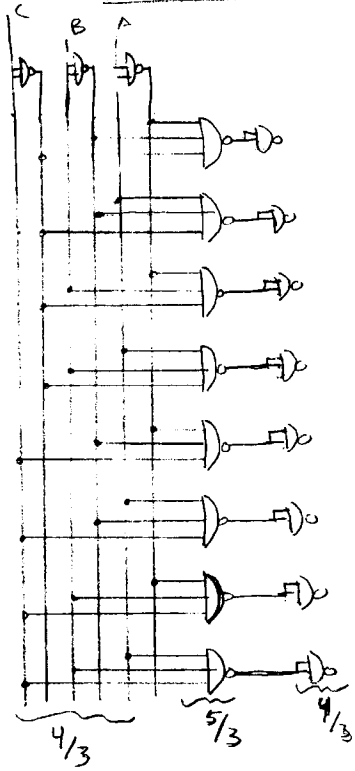
4-2) Logical Effort of 3-Input Nor Gate = $7/3$



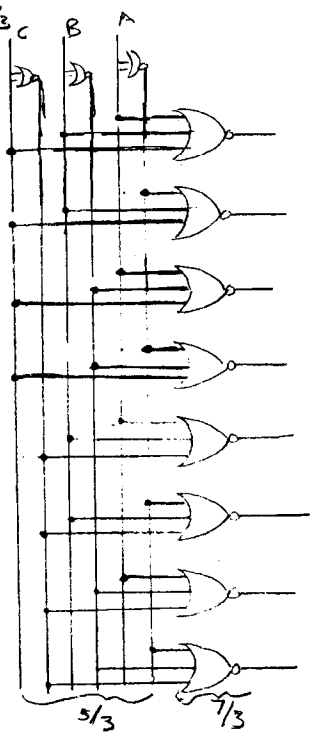
⇒ Capacitance is (6+1) Cunit for a 3 input Nor Gate

⇒ capacitance is (2+1) Cunit for an inverter

4-3

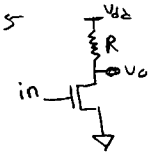


g = $7/3$



Note the total logical effort with the nor gates is smaller because there is 1 fewer stages.

4-5



$\Rightarrow$ output rising: $T_{50\%} = 0.64\, R C_L = T_{LH}$ where C_L is the input capacitance of the next gate

$\Rightarrow$ output falling: Assume V_o goes from $V_{dd} \rightarrow V_{dd}/2$

When $V_o = V_{dd} \Rightarrow I_R = 0$

$I_T = \frac{1}{2} K_n \frac{W}{L} (V_{DD} - V_T)^2$

When $V_o = V_{dd}/2$ Assume transistor is in linear region

$I_R = \frac{V_{dd}}{2}\left(\frac{1}{R}\right)$

$I_T = K_n \frac{W}{L}\left[(V_{DD} - V_T) V_{dd} - \frac{V_{dd}^2}{2}\right]$ Transistor Current

$I_{avg} = \dfrac{\frac{1}{2} K_n \frac{W}{L}(V_{DD} - V_T)^2 + \overbrace{\left[K_n \frac{W}{L}(V_{dd} - V_T)\frac{V_{dd}}{2} - \frac{V_{dd}^2}{2(2)}\right] - \frac{V_{dd}}{2R}}^{\text{Resistor Current}}}{2}$

Assum $K_n \frac{W}{L}\left(V_{dd} - V_T\right)\frac{V_{dd}}{2} - \frac{V_{dd}^2}{2(2)}\Big) \simeq \frac{1}{2} K_n \frac{W}{L}(V_{DD} - V_T)^2$

$I_{avg} = K_n \frac{W}{L}(V_{DD} - V_T)^2 - \frac{V_{dd}}{2R}$

$\Delta t = \frac{C \Delta V}{I_{avg}} = C_L \frac{V_{dd}}{2}\left[\frac{2}{K_n \frac{W}{L}(V_{DD} - V_T)^2 - \frac{V_{dd}}{2R}}\right]$

$T_{HL} = \dfrac{C_L V_{dd}}{K_n \frac{W}{L}(V_{DD} - V_T)^2 - \frac{V_{dd}}{2R}}$

CMOS:

$R \simeq 10\, R_{nmos}$

So, If we replace R by a pMOS and assume $\frac{W_p}{L_p} = 2\frac{W_n}{L_n}$ and that $R_{nmos} \cong R_{pmos}$

$\Rightarrow$ output Rising

Load Capacitance $\Rightarrow 3C_L$

Resistance $\Rightarrow$ 1/10 R

$T_{50\%} \simeq 0.69\, 3C_L \frac{R}{10} \Rightarrow \frac{3}{10} 0.69\, R C_L$

$\Rightarrow$ Has about 30% the rise time of the Pseudo-nmos inverter

$\Rightarrow$ the T_{HL} time is simply

$\simeq \dfrac{C_L V_{dd}}{K_n \frac{W}{L}(V_{DD} - V_T)^2}$

$\Rightarrow$ Predicts about 90% the fall time

Also, there is no static power dissipation