

ECE 124a/256c

Advanced VLSI Design

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Forrest Brewer



# Course Logistics

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- 8 Homework assignments (20%)
  - Out Wednesday, Due following Wed. before Lecture
- 8 Quizzes (20 minutes each drop low score) (30%)
  - Friday or Recitation starting 2<sup>nd</sup> Week
  - Topics from homework, cumulative
- 4 Labs (50%)
  - 1-2 weeks as required
  - Last Lab is often small project, due at time of final schedule
- 1 page of notes for quiz and finals
  - This is important... Not the using – the creating!



# Course Content

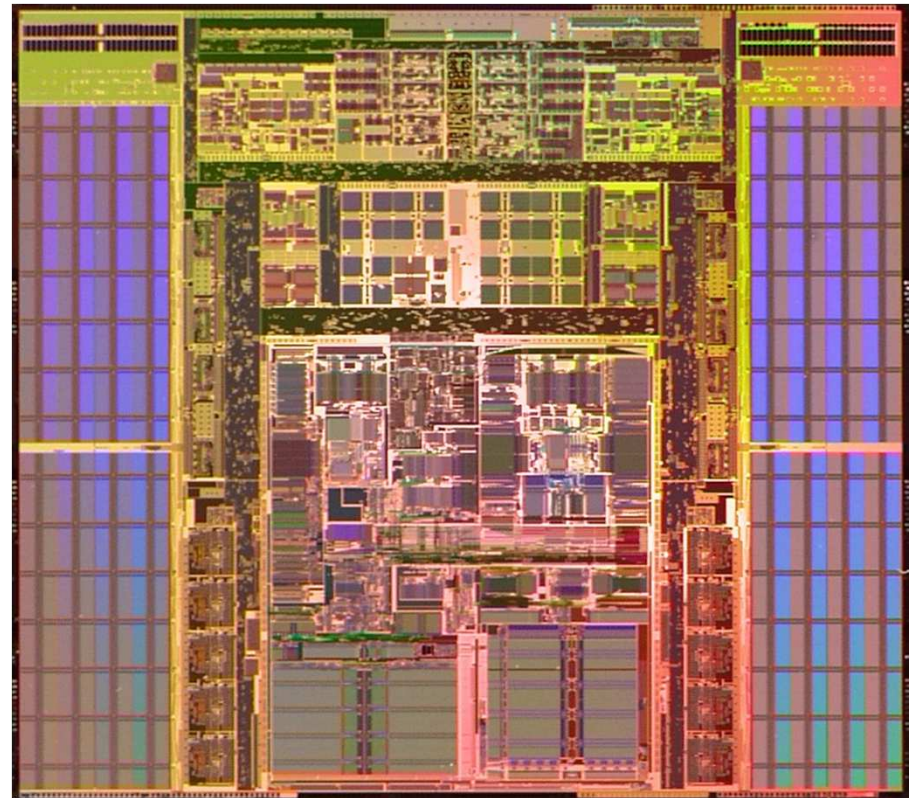
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Practical Issues in VLSI Design: (the often forgotten physical limits and issues)

- Noise – digital paradigm
- Signaling – on and off die
- Wires – lumped, RC and transmission lines
- Synchronization
- Power
- Packaging (board issues)
- Latency and Coherence (Performance)

# VLSI Architecture

- Architecture is organization of Control and Operative parts
- Wires, delay, organization of data motion vs. power and noise limits
- Spatial Organization of Design: Floorplanning, Design Regularity
- How can you tell this is a processor?





# VLSI System Engineering

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- 2 of 3 startups fail to deliver a working part
  - 50% of those that do fail to meet expectations
  - 90% take longer than expected
- NRE (non-recoverable-expense) is growing
  - \$800K for single 90nm bulk CMOS mask set
    - \$250k for single 35nm phase mask (25-35 needed!)
  - Can not make several spins to get it working!
- Digital Packaging is now Microwave Design
  - 10 GHz serial I/O commonplace
  - Boards can have several clock cycles of wire delay



## Failed Company (\$58 Million Invested)

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- Custom Processor Design in Vanilla CMOS (2000 at 0.15um)
  - 8.5 million gates
  - 26 Watts
  - 1296 pins / 785 signal pins
  - Design took 2 years longer than expected
    - Timing closure
    - Interface design and debugging
    - Packaging required special pad driver design
  - Required 121pS jitter limit across entire die
- Market window evaporated— Lost opportunity

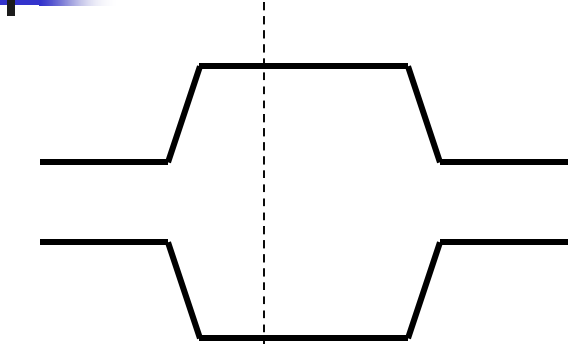


# Aim of Course

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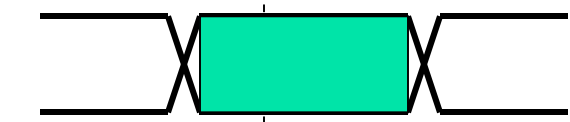
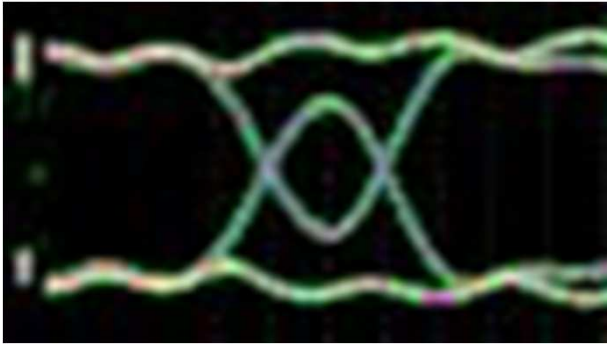
- What are the physical issues that lead to design organization and architectural tradeoffs?
- How to engineer high-quality designs
  - Why faster logic may not lead to faster design
  - Why power is inexorably linked to performance
  - Why clock trees get smaller (and latency gets larger) with increasing performance
  - Why Intel spent 8 billion on package technology – and it is over half the total cost of producing a high-end commodity processor
  - How to look for game changing possibilities in the future

# Eye Diagram

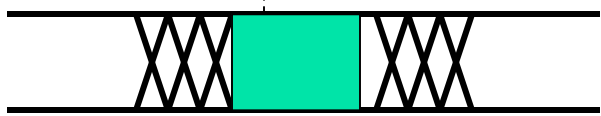


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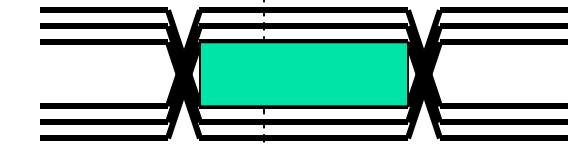
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Eye (Safe signaling clearance)



Timing Noise (Jitter)



Level Noise

Sample Point





# Noise

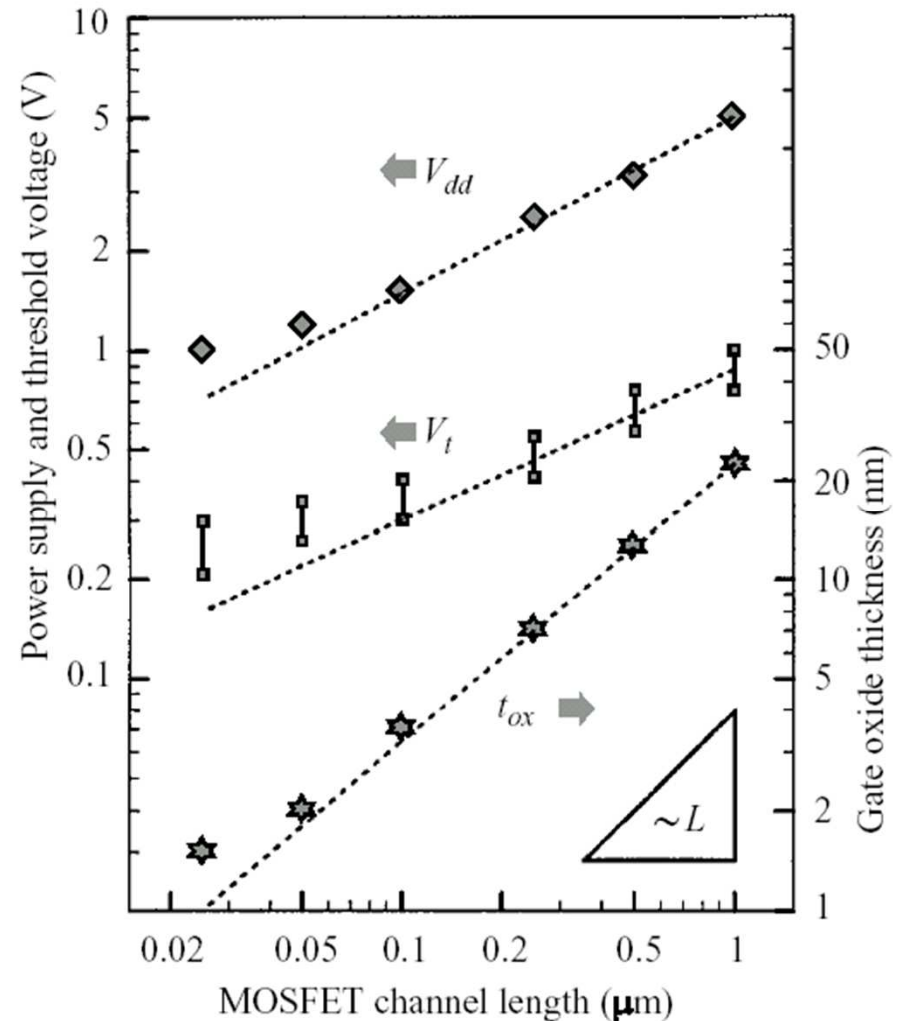
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- Power Coupled Noise:  $L \, di/dt + IR$
- Substrate Noise
- Capacitive and Inductive Signal Coupling
- Thermal Noise ( and sub-threshold conduction)
- Induced timing variation
- Device Variability

All noise sources act to decrease Eye size (available signaling margins) – noise sources cannot be eliminated so must be *budgeted*.

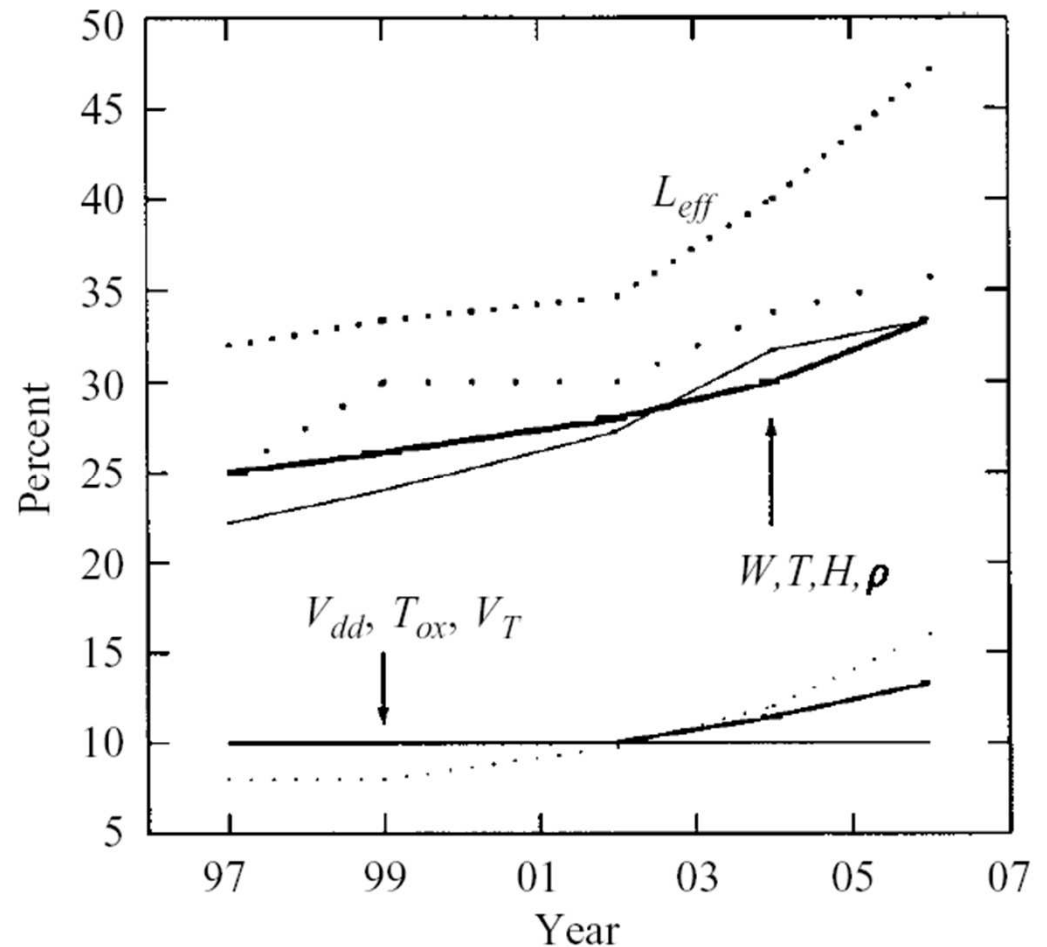
# MOS Device Scaling

- Decreasing device sizes reduce parasitic loads making for faster transitions
- Increase variations between devices and across the die
- Shrinking supply voltages increase noise sensitivity and reduce margins
- System performance limited by noise and clock skew (jitter)

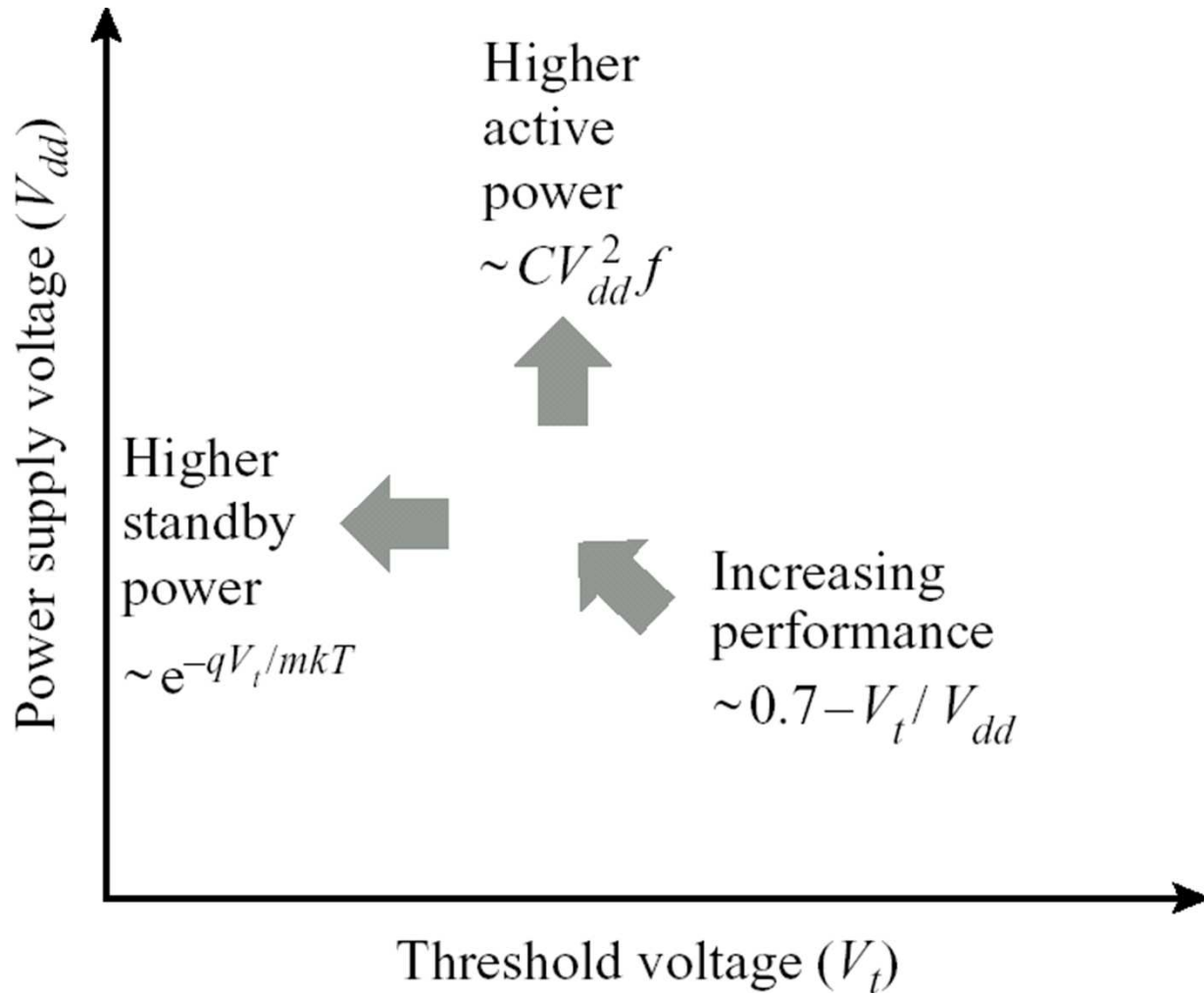


# Device and Interconnect Variation

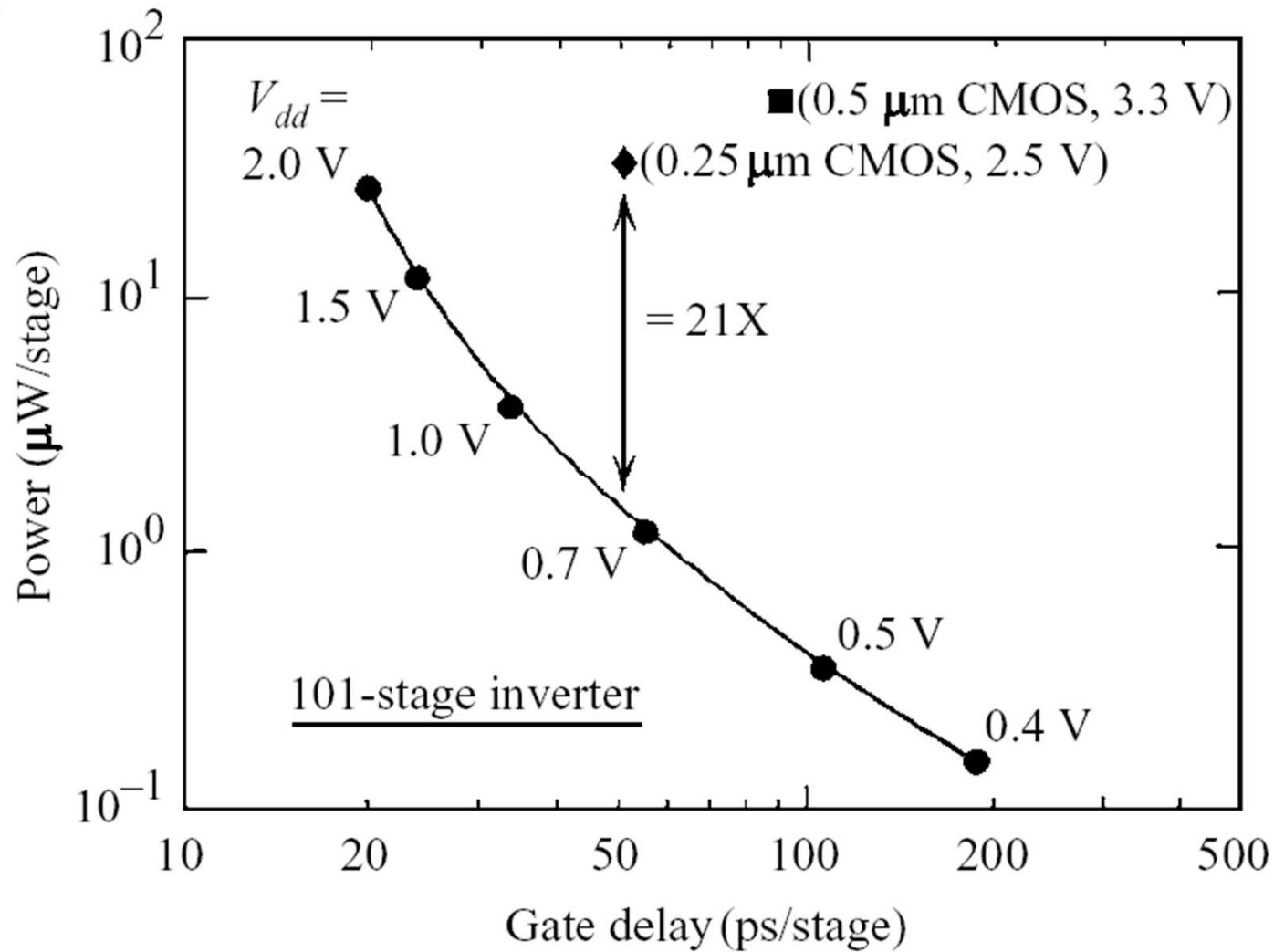
- Scaling induces increase in magnitude of device to device variations
- Note particularly large increase in  $L_{eff} \Rightarrow$  MOS current



# V<sub>dd</sub> and V<sub>t</sub> changes

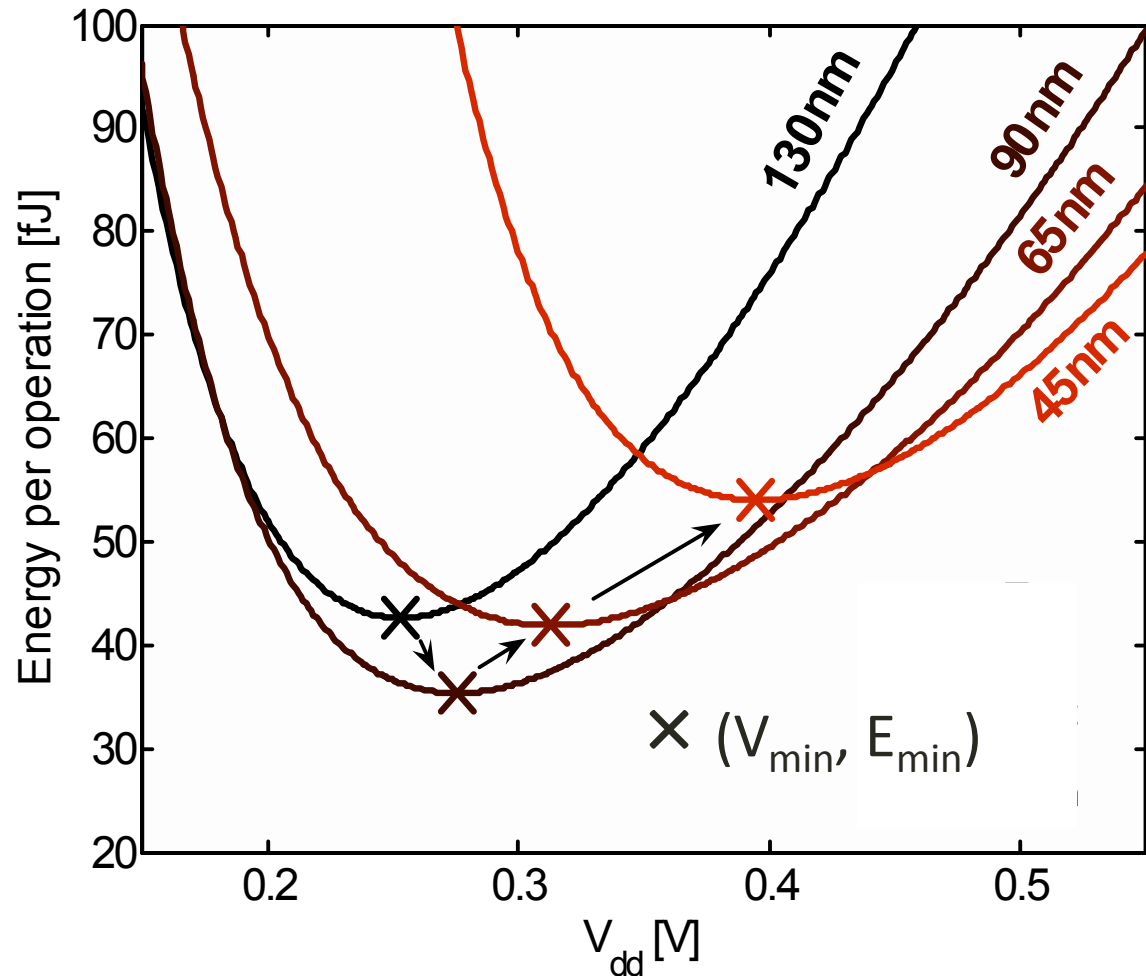


# 100nm Ring Oscillator



# Practical Energy Scaling

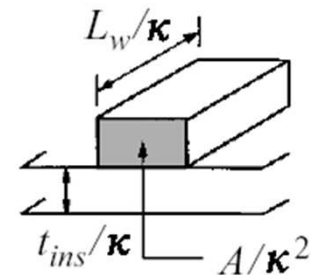
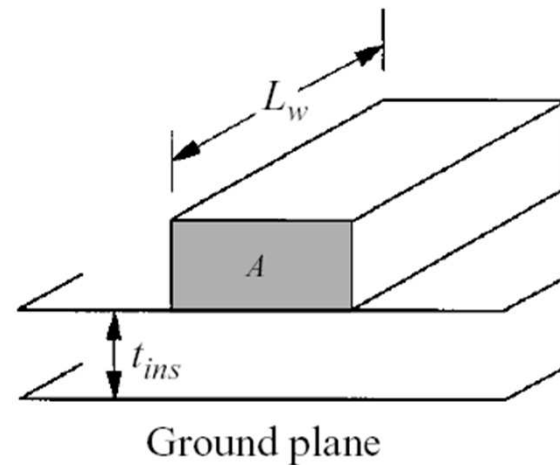
- 8x8 mpy
- Analysis includes DIBL and variation effects
- Leakage from low  $V_t$  variants dominate power



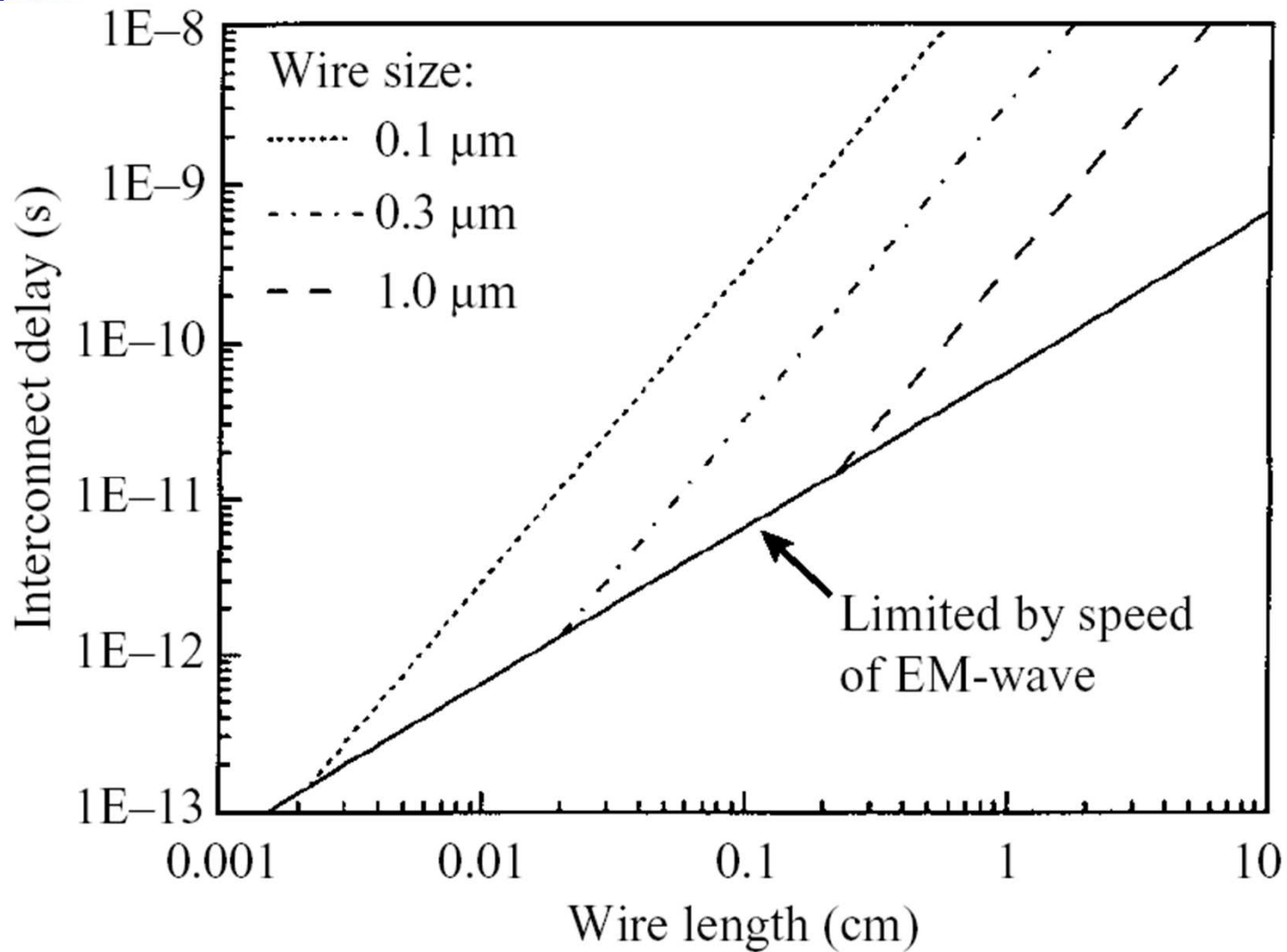
(D. Bol 2009)

# Wire Scaling

- Wire Resistance grows as the square of scale decrease
- Wire Capacitance is nearly constant with scaling!
- RC delay increases rapidly with feature size scaling—  
Dominates delay of long wires



# RC delay vs. wire-length





# Intel 45nm micro-processor interconnect

- Cu Wiring
- Low-k ILD
- Narrow plugs
- Stacked vias
- Note aspect ratio and wire spacing!

M8

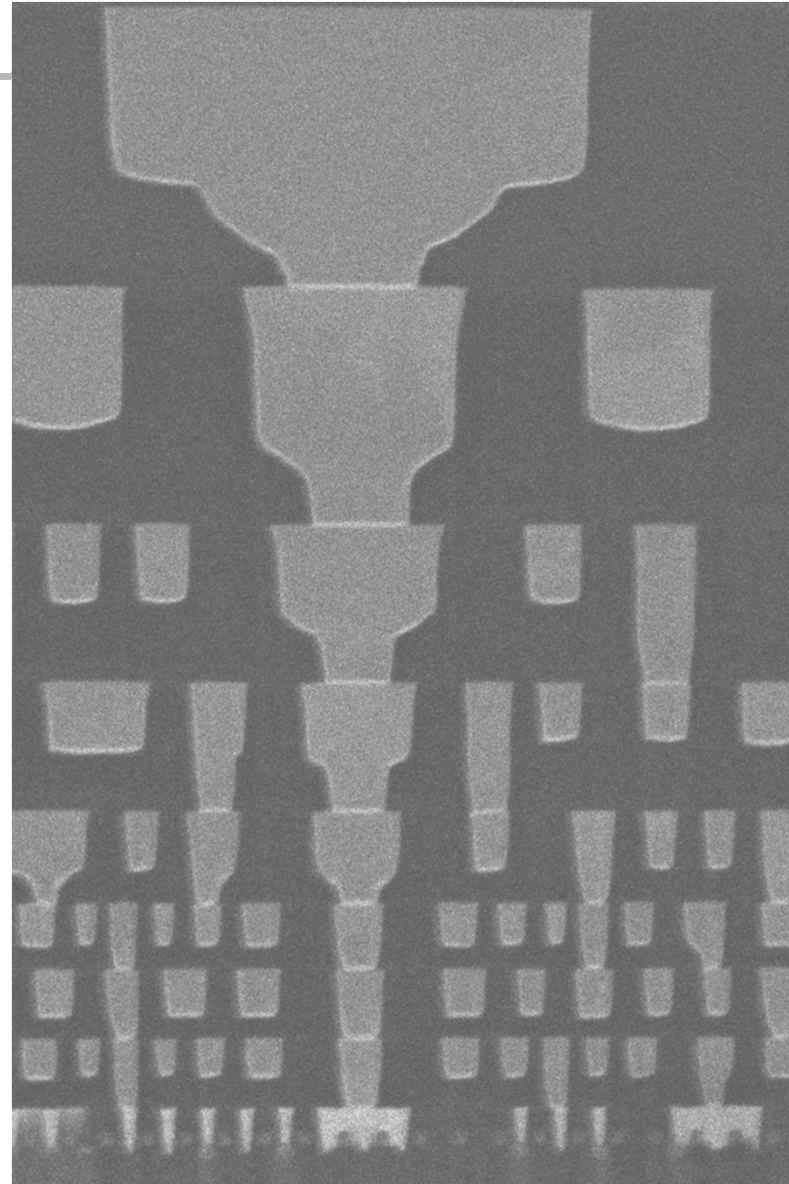
M7

M6

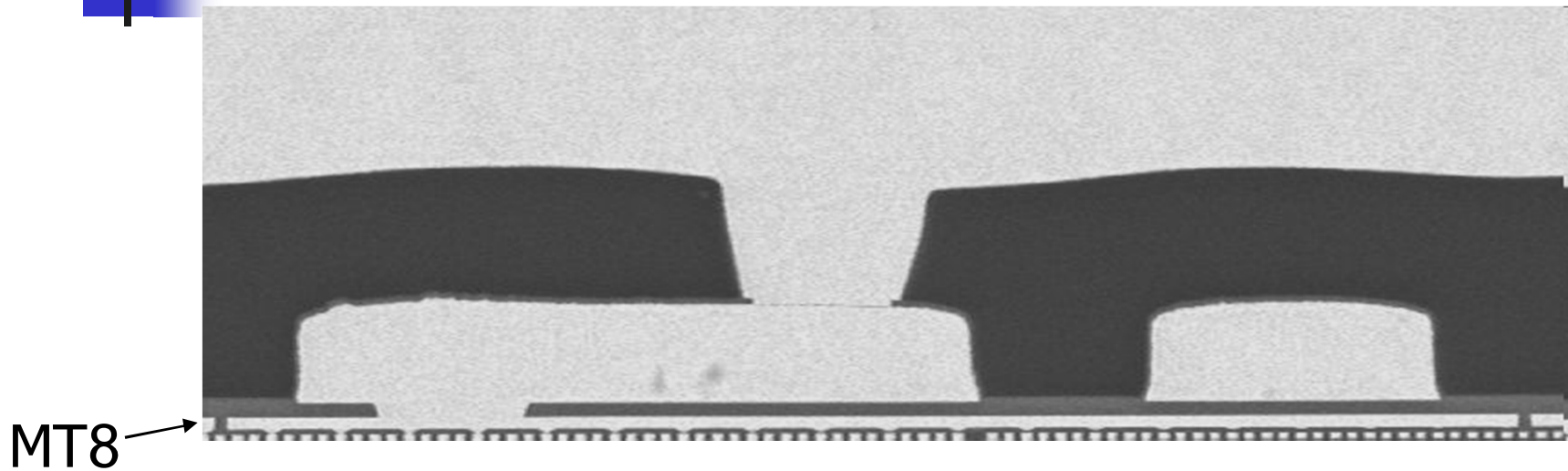
M5

M4

M1-M3



## Intel 45nm Power Level



- Added 7um thick Power redistribution layer MT9
- Huge layer needed to lower power coupled noise caused by dynamic Vdd switching



# Interconnection Latency

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The distributed RC delays in long wires force changes in the architecture of the chip:

- Clocking and clock distribution
- Clock domains
- Pipelined Control
- Feed-forward data-flow



# Timing Skew

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- Large delays and latencies also increase timing variations
  - How can you be sure that clocks and data arrive properly
  - Eg. Flip-flop to flip-flop connection can be problematic
- Synchronous Islands
  - Clock domains are forced by the cost of limiting clock skew given high impedance wires
  - Mandatory re-synchronization of signals crossing clocking boundary
- Jitter (uncorrectable timing variation) provides limit on system performance



# Power Distribution

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- Large VLSI chips use astonishing amounts of power
  - Pentium 4 had peak current draw of 85A @1.2V
  - Worse, on-chip demand at 250pS rise-time
  - Off-chip power is decoupled, but still can rise in <2nS
  - What is the effect on package inductance?

$$V_{\text{drop}} = L_{\text{package}} \, dl/dt = 85\text{A}/2.0\text{nS} = 43 \text{ V/nH}$$

A typical package pin has 8nH of inductance...



## Next Time

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- Electrical Properties of Wires
- R/RC and RLC models