Lab 5: Latch Characterization

Due Wed. Feb. 27

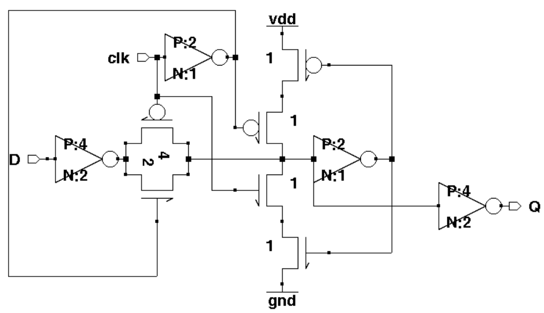

Figure 1. MMI latch design

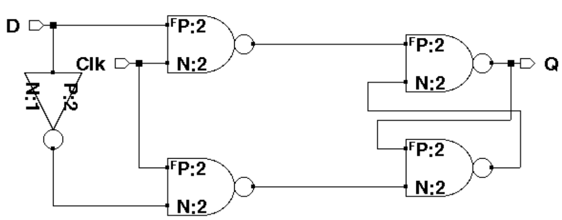

Figure 2. NAND Latch

I. Background

Latches, while a common component in VLSI design, pose a challenge for characterization. The function of a latch is to hold data for an externally determined time. This function is a common one used when synchronizing signals. In typical synchronous design all signals need to be synchronized to a clock. This causes latches to be used extensively in such circuits. Because latches make up such a significant part of the circuitry on a chip, optimizing the behavior of the latches used can greatly impact the performance of a given design. In this lab you will be asked to characterize two kinds of latches and their behavior under variation.

II. Circuits

This lab focuses on two latching circuits. The first latch to investigate is the latch that MMI offers in the extracted cell library posted on the website. (This is the most common type of latch in vanilla CMOS design as it has interesting hold delay properties. A rough circuit diagram for this latch can be seen in Fig. 1 . The other latch we will concider is one typically shown in beginning digital design text books. This latch design can be seen in Fig. 2 . Since we don't have an extracted version of this latch, you will need to make one out of the extracted nand gates.

Parameter	Nominal	1 sigma variance
VDD	1.3v	.2v
GND	0v	.15v
lp_min	180nm	18nm
ln_min	180nm	18nm
C	*	.2fF

Figure 3. Parameters to vary

III. Characterization

The characterization process for a latch is a little more complicated than the one for the nand gate we saw in the previous lab. While the latch has the same number of inputs and outputs as the nand gate, the relative timing of these inputs is crucial. We are interested in the following parameters for a latch are: clock to Q delay, D to Q delay, setup time, hold time, and timing aperture. The first two measurements are similar to the propagation delay that you measured in the previous lab. Clock to Q measures the time for the output to change to a new value when the clock goes from latched to transparent modes for both rising and falling transitions. D to Q is measured in the transparent mode of the clock. The next three parameters are all timing relative. The setup time is the amount of time for which the data has to be stable before the latching clock edge in order to guarantee proper function. The hold time is the amount of time after the clock edge the data has to be stable for, to ensure that the state does not change. The timing aperture is the time from the beginning of the setup time to the end of the hold time. Note that it is possible for hold times to be negative! Since these extractions were done against a .18u technology, use the .18u transistor models when characterizing these gates. VDD should be 1.8V for these runs. It is often convenient to measure flip-flops and latches using 2 non-comsurate clocks at slightly different frequencies – so that the relative phase drifts slowly and thus every combination of setup and hold is measured in a single run. As always, drive the inputs and outputs of your circuits with intelligent selections of CMOS drives and loads.

IV. Characterization Under Variation

Repeat the characterization process using Monte Carlo simulation. vary the following parameters by the amounts shown in Fig.3 . In addition to these variables create a modified version of the extracted models and have their parasitic capacitances vary by .2fF at 1 sigma. Report the extrema, 1 sigma and average values for these runs.