

# ECE 124d/256c

## Final Lab: “Clock Network Design”

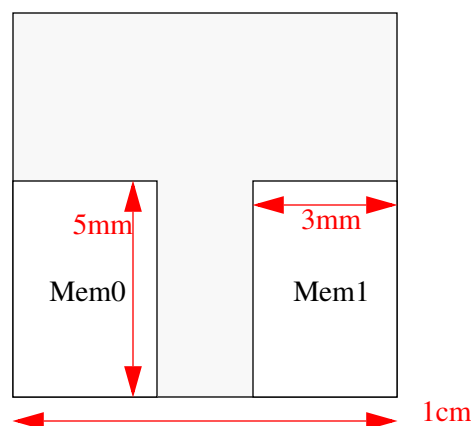
- Due: Tuesday March 18, 2008 at final

In this lab, your job is to design a single phase 200MHz clock tree suitable for driving 200,000 flip-flops which are uniformly distributed over a limited region of a  $1\text{cm}^2$  die as shown in the figure below. Since there are 2 large memories in this design, you need to provide clocks only to the remaining T-shaped region, and the flip-flops are uniform over this region. Each flip-flop has a  $6\text{fF}$  load on its clock input and your clock needs to have a single source which you can assume has zero jitter and is modeled by a single MMI\_INVE gate driven by your (perfect) clock (use a  $60\text{pS}$  rise and fall voltage source for the input to this driver).

You are using metal interconnect with a resistance of  $45\text{m}\Omega/\text{sq.}$ ,  $40\text{ aF}/\mu\text{m}^2$  area capacitance and  $65\text{ aF}/\mu\text{m}$  fringing capacitance on each side. The total cap = area component + 2 times the fringe component. (This specification is so you can make the wire wider and have a reasonable estimation of the capacitance and resistance. You may use up to 3 layers of metal in the clock tree, and can make the wires as long and wide as you desire). You will need to incorporate vias in your design, each metal to metal via will have 1 ohm of resistance. A 3 resistor+ 2 capacitor pi-model is sufficient to model each of the wire segments in this design. You need the delivered clock rise time to be less than  $150\text{pS}$  and the maximum skew+jitter to be less than  $1.5\text{nS}$  at the terminals for both rising and falling edges. Note that the clock delay can be several times this value. The system is subject to jitter because all of the buffers derive power which has a maximum droop of  $180\text{mV}$  ( $1.8\text{ V}$  nominal,  $1.62\text{ V}$  minimum). Show how you model the noise in your design which is conventionally wire bonded on the edge (so that you can assume that power and ground noise is usually coupled and anti-symmetric).

Your buffers are selected from the MMI\_INV(A-E) inverters which can be used in any number (or in parallel) in your design. ((This means you can make 2-gate non-inverting repeaters from the inverters -- the trade-off is longer delay, higher power, but you might get better skew buildup performance). However, your goal is to minimize the power dissipation of your clock network at 200MHz. Thus wider wires (lowering the resistance), add capacitance and may cost you power as does adding more inverters as clock repeaters. The goal in this lab is how low a power dissipation you can achieve while still meeting the desired skew, jitter and rise/fall time goals.

Although you can place the inverter repeaters anywhere, you need an even number on each path from the source to each flip-flop to make sure the clock has the same phase everywhere. Since you cannot build the entire circuit (it would simulate much too slowly), you need to exploit symmetry in the design



design so that the number of unique segments is minimized. Then you only need to simulate the uniquely different paths as long as you adequately add capacitive loading to the tree terminals to represent the tree segments you are not simulating. Design of this model is the primary effort in this lab -- please justify the assumptions you make and the sizes of parasitics and ensure that your tree covers all of the needed flip-flop terminals. (If you choose a spanning tree instead of an H-tree to lower the power in some part of the design, build both upper and lower bound distances as two different paths). To find the total power, measure the current each buffer is using and multiply by the number of similar components if all the clock tree was built.

While it is possible to build a very simple network to meet the above goals, getting minimal power is tricky. Please discuss the methods you use and results you obtain for your design clearly. This is the last lab in the class, and will be graded most carefully. You will need to describe the layout of your network, showing specific lengths and widths at each level of the tree as well as the number of buffers and the capacitor loads to represent the other clock paths branching away. Also show the models you used for the wire resistance and capacitance and any minimization techniques you tried. For the purposes of this lab -- you cannot add additional PLL clock generators unless you can justify their power and performance models -- i.e. if you want em -- you gotta build em.