ECE 124d/256c
Lab 5: Power Bypass Design

One week. In this lab, it is you against the power coupled noise. You have a set of capacitors to use on the package and you need to find a bypass solution that keeps the power noise below 10% on each power rail over the relevant time period. Your capacitors can be selected from the following varieties. Note that for the smaller types, the cost is solely dependent on the packaging option, as is the inductance.

Table 1: Capacitors

Value	Type	ESR	$	L
10pF	NPO	0.01	0.05, 0.20, 2	1.2n, 650p, 120p
100pF	NPO	0.01	0.05, 0.20, 2	1.2n, 650p, 120p
1nF	NPO	0.01	0.10, 0.40, 2	1.2n, 650p, 120p
3nF	X7R	0.5	0.5, 0.20, 2	1.2n, 650p, 120p
30nF	X7R	0.5	0.10, 0.40	1.2n, 650p
300nF	X7R	0.5	0.10, 0.40	1.2n, 650p
5uf	Tant	0.05	0.30	2nH

You also have the option of adding on-chip bypass area capacitance. Because of package pad issues, you get 70nF on chip for free, but adding additional on-chip bypass adds to the chip area and thus reduces the number of die you get from a wafer. For this chip, an additional 10nF uses $5mm^2$, adding to the $65mm^2$ minimum. In the minimum size, you get 654 die per $1,500 wafer. Adding to the area, you get proportionally fewer chips -- but the wafer cost is fixed so your price per chip goes up. This chip is packaged in an epoxy package with a cost of $4 each in large quantity. Finally, you pay $0.05 per device for place assembly charges on the package. Your goal is to minimize the cost of a working package/chip combination.

To simplify the problem, you only need design the package bypass capacitors for the package itself (C1) in the figure and the value of the on-chip bypass (C2) capacitance you used. For the on-chip bypass, you can assume an ideal capacitor, but use the realistic series model (inductance and resistance in series with the ideal capacitor) for each capacitor you add to the package, filing in the inductance and resistance from the package choice you made. You will need to have several capacitors of different sizes to meet the 180mV maximum deviation over the wide range of frequencies. Be sure to simulate the circuit for at least 50uS to be sure you have captured all the behaviors, however, you will need enough resolution to capture the high frequency behavior of the current sources. Neglect undershoot during the first 1uS of turn on, but you can never have overshoots in execess of 10% of Vdd. This is a lab in which you might want to use measure statements instead of storing all the node voltages, to reduce space usage. For your convenience, I have provided lab5.sue and lab5.sp files on the course website.

As always, describe your methods (even if you guessed or trial and error) and show the final schematic and results on the terminals Vvdd and Vgnd. Remember that widely different sized capacitors have applications in different frequency regimes. Also, note that Idc packages are quite expensive, but might still be cost effective. (There is also a physical size issue which we are ignoring here). There are several short papers on the website with procedures for designing bypass networks, be sure to take a look before blindly pluggingin too many trials. One approach is to divide up the frequency bandwidth into a set of bands corresponding to the effective bypass bandwidth of the capacitors and determining cost effective solution points. (i.e. you can trivally find a solution by adding a lot of on-chip decoupling -- but this is very expensive for low frequencies even though it is essential for the high frequency events.)