# ECE 124d
# Lab 4

1 week: This lab has 2 parts -- in both parts you are examining the behavior of circuits given a noisy environment, namely, power coupled noise.

## Part 1

Using the fast repeater circuit you built for Lab 2b, instrument the spice deck so that you have separate power and ground connections for each inverter/repeater. Do this by making the power and ground connections of your cells available if you used sub-circuits and then add separate power and ground voltage sources to each buffer, all referenced to node 0. (Do not vary the ground terminals you used in your wire models-- you don't know where they have been!) Characterize the total line delay variation when the Vdd and Gnd sources both have 10% deviations from nominal values. For the .130um technology that means that Vdd will be between 1.17V and 1.43V Gnd will be between -0.13V and 0.13V. Assume no correlations between the variations (i.e. each of the voltages is varying independently, for each of the repeaters). Measure the delay from input to 50% of Nominal Vdd at the input of each inverter in your design for several different cases of voltages to determine delay variation from nominal as a function of distance from the wire source. This task can be greatly sped up by using the .MEASURE and .DATA statements in hspice. Effectively, .MEASURE can be used to find the delay alone and each line of .DATA can be used to set the voltages of all of your sources. You do not need to exhaustively simulate all cases, 30-50 test cases is enough to get a good idea if the cases are chosen carefully. Alternatively, you can use the built-in Monte-Carlo distribution parameter funcitions in HSPICE -- but keep the simulation times to a few minutes, max. Your results should be interpreted in terms of the total variation and the incremental variations added by each driver segment. Can the total delay decrease from the nominal one, despite the power variations which only reduce the local Gnd-Vdd difference at each inverter? If so, why? How do the 45nm results compare to the 130nm version? Are the delay deviations in proportion to the voltage of the scaled process?

## Part 2

a. In part 2, you are to characterize the 'delay' of the MMI_NAND2B gate (use the extracted spice deck from the web site, and 0.18um transistror technology). There are 16 possible input transitions on 2 inputs, of these only 6 cases change the output of the NAND. Find the 50% delay from input to output for each case, where the inputs are driven by MMI_INVA gates and the output is loaded by a capacitance of (5fF, 10fF, 20fF) power at (-10%, nominal and +10%) power supply levels. Fit delay versus load lines for the rising and falling output cases.
b. Then, carefully measure the instantaneous current to determine the peak current, total charge, and typical power pulse width used in this gate for rising and falling transitions.