

ECE 124d/256c: Lab 3 Buffer Insertion

Due 1 week (Wed 2/13/2008)

In this lab, you will characterize the properties of practical buffer insertion in a realistic wire model, set in 130nm and 45nm technologies. For this purpose, you will design a solution, build the model, simulate results in spice to both check your results and determine the characteristics of your design. We are modeling mid-size wires in each technology, with the expectation that they will be surrounded by more wires on all 4 sides. In such a case, a conservative modeler would put a ground plane above and below the wire as well as place wires at minimum spacing from each other. This results in the following wire parameters:

Table 1: Wire Parameters

Tech	Vdd	width	space	thick	ILD	k	R/mm	L/mm	C _T /mm	C _C /mm
45nm	0.9V	120nm	120nm	350nm	150nm	2.2	523	1.7nH	186fF	63fF
130nm	1.3V	280nm	280nm	450nm	450nm	3.0	174	1.7nH	180fF	56fF

Note: space is the inter-wire separation, ILD is the separation between vertical layers Ct ia the total and Cc is the adjacent coupling capacitance. The inverter minimum size n transistor and parasitic parameters are shown below:

Table 2: Inverter Parameters

Tech	ln_min lp_min	Wn min	sdd (um)
45nm	45nm	90nm	0.2
130nm	130nm	220	0.5

You need to build models which generate reasonable AS, AD, PS, and PD parameters for your spice deck, it is simplest to use a custom header (modified from the 0.18um version on the class website). Be sure to update the parameters (like Vpp/Vdd) accordingly. 'sdd' refers to the expected distance from the gate to the far edge of a contacted source or drain region and is used to estimate source and drain area and perimeters, Wn is the minimum inverter n-channel size, choose an appropriate p-channel width to get roughly equal rise and fall times for the inverter. You will need to build much larger inverters, for convenience, let the minimum size be denoted as 1X, larger sizes scaled in terms of this size.

Your goal is to deliver the output of a 40pS rising edge into a 1X inverter to the input of another 1X inverter located 5mm away with the smallest possible delay, measured from the 50% points of the input of the first 1X to the 50% point of the output of the end 1X. You can insert inverters of any scaled size at any position between these entry and exit points, but cannot change the wire parameters. Find and plot the peak currents for your inverters, describe the sizes, the link delays, propagation delay of the link per mm and worst case slope at 50% swing for each case. Do not worry about the phase of the edge (i.e. whether the output is rising or falling). Lastly, propagate a 200pS wide pulse through your link in both technologies. Does the pulse see the same delay as the rising edge? What happens to the pulse width?