

ECE 124d/256c

Lab1 (part b)

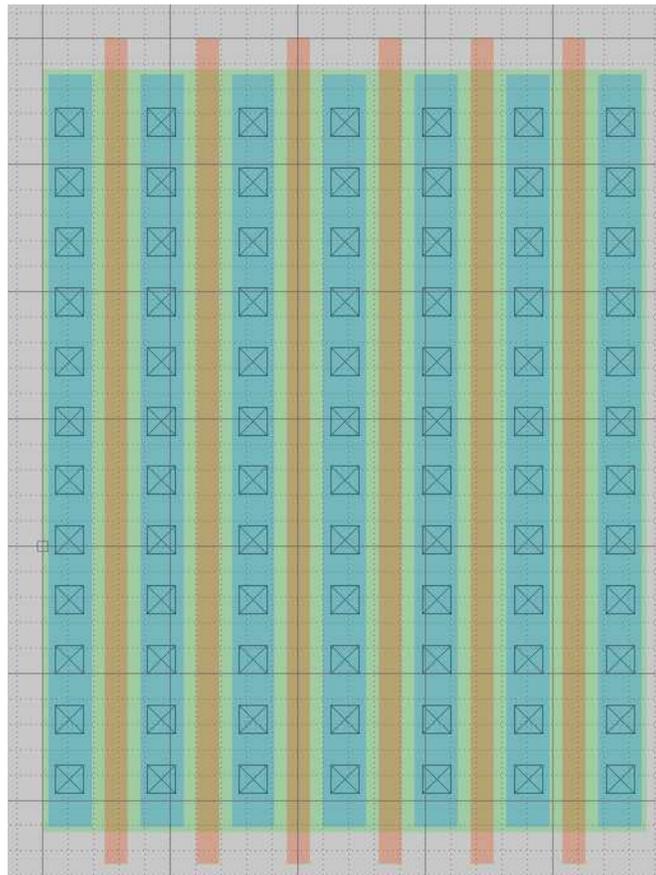
Due: Wed Jan. 19, 2011 (1 week)

In this lab, we will explore the coupling of CMOS inverters as drivers and receivers for transmission lines. For this lab, we will use the PTM synthetic models which are academic mock-ups that do not require NDA signatures for release. You will also need the PC-board wire models you designed for lab1 part a.

Exp1:

First, you will need to characterize the driver characteristics and loaded inverter behavior. We will assume that your drivers are built out of thin oxide transistors for this exercise -- in practice, you'd likely use thick oxide ones for higher driver voltages, so we'll drive the interface at 1.8V for the standard 0.18um devices.

Construct a CMOS inverter with 0.18x36um n-channel and 0.18x48um p-channel transistors. Be sure to include appropriate source and drain area and perimeter figures using the minimal $sdd=0.48\mu\text{m}$. (sdd describes the minimum thickness of a contacted source or drain region -- the width is set by the transistor width). In fact, the device will most likely resemble the picture below:



In practice, all the gates are tied together and source/drain regions alternate to get a dense, parallel-transistor layout. The end extension is $s_{dd}=0.48\mu\text{m}$ and the inter-gate distance is $0.54\mu\text{m}$. This arrangement is called a matrix transistor and the above parallel transistor has a total width of $36\mu\text{m}$. It is best to model such an arrangement as 6 parallel transistors with identical widths and lengths and nearly identical source and drain area/perimeters. Technically, the perimeter is used to determine the sidewall capacitance -- which occurs between the diffusion and the channel stop. In a matrix transistor, the diffusion regions are merged so that the perimeter is very limited -- in the transistor above, there is only $2 \times 0.54\mu\text{m}$ segments of perimeter on the internal transistors. Since the source and drain contacts are shared between two transistors, it is common practice to split the area and drain spice parasitics (AS/AD, PS/PD) between the two sharing transistors. In this technology, similar spacing applies to the p-channel transistors as well. Use these facts to build a spice model of the matrix transistor based inverter driver.

Now characterize the driver, for rise and fall swing parameters: input and output capacitance as well as average drive capability at the 1.8V supply level for 20%-80% and 0%-50% swings. Input and output capacitances include non-linear components so you'll need to determine the equivalent capacitance over the swings above: $C_{eq} = \Delta Q / \Delta V$. There are several ways to find ΔQ -- the most direct is to integrate the instantaneous current into the model, however, a simpler method is to place a suitable resistor in series between an abrupt swing source and the transistor input. Then you can measure the charge time for the required swing to determine the effective RC_{eq} . It is a good idea to use a few different resistances covering the typical observed rise and fall times of a given technology to build statistics for the measurement. ($0.18\mu\text{m}$ technology at 1.8V has rise/fall times between 25-175pS for high perf loadings).

To measure the output/internal capacitance and drive capability, measure the rise/fall times for 20%-80% and 0%-50% swings into a capacitive load. Again, select appropriate loads for the expected rise/fall times. Here you are driving output pads and pins and TM lines -- so you should expect loads on the scale of 1-5pF. Plot the capacitance vs. swing delay to determine the swing averaged current and effective output resistance. Use at least 5 trial loading capacitances. Note that the delay has a non-zero projected value even for zero loading. This internal loading captures output and several internal parasitics.

In any simulation of a transistor circuit, you must always consider the finite output resistance or current capacity of the circuit's input. It is common practice to insert a resistor limiting the current from a PWL source before the input of any gate simulation. Alternatively, using an inverter similar to the expected input drive capability is a good idea. In either case, choose the size to guarantee a rise/fall transition that is close to the expected circuit behavior. (Here assume a 50pS 0-50% swing). In future labs, always consider the input loading requirements in your simulations.

Exp 2:

Using the data from above, calculate the widths for P and N necessary to source terminate the PC board TM line from Lab 1a. Plot the voltage at the driver, midpoint and endpoint of a 2cm long TM trace to verify that the line is indeed source terminated.

Investigate the behavior of a small series inductor placed at the midpoint of the TM line -- use 4nH. Also try a parallel capacitor of 1pF at the same location. Do the results follow your expectations?

Finally, build a model of a simple package pin-TM-pin system by adding a 3nH series inductor

followed by a 2pF cap to ground, then the TM line (2cm), then another 2pF cap to ground, another 3nH series inductor and a final 1pF cap to ground. Measure the noise across this final cap to approximate the signal noise at the line far end. Considering that typical signal noise limits are 10% of Vdd -- is the noise substantive?