On Chip Power Distribution

* CMOS Devices have very uneven power draw \( \Rightarrow I_{\text{peak}} >> I_{\text{avg}} \) for typical design.

E.G. Consider a 0.35\( \mu \)M inverter driving 2 other inverters w. 200\( \mu \)M of wire:

\[
\omega_p = 4\mu m \quad \omega_n = 2\mu m \quad \text{Total load } \sim 62fF
\]

\[
V_{cc} = 2.0V \Rightarrow Q_{ch} = C_L \cdot V_{CL} = 124fC
\]

Given \( R_{chN} \sim 10K\Omega \) @ 0.35\( \mu \)m = \( L \)

we get: 1.14mA peak current (\( I_{\text{dsat}} \))

\[
\Rightarrow T_R = 100pS
\]

given input rise time of 200pS we expect ~ 200pS 0-90% rise as well, similar fall since 2x width. (Actual = 240pS)

Wave forms:
On Chip Power Distribution

Typical current pulse is triangle with base \( = 2T_R = 2T_P \).

Peak current is convolution of input rise/fall and output rise fall:

\[
I_{\text{peak}} = \begin{cases} 
0.75 \cdot I_{\text{dsat}} & t_{\text{in}} = t_{\text{out}} \\
1.0 \cdot I_{\text{dsat}} & t_{\text{in}} \ll t_{\text{out}} \\
0.5 \cdot I_{\text{dsat}} & t_{\text{in}} \gg t_{\text{out}} 
\end{cases}
\]

- On the other hand \( I_{\text{avg}} = \frac{K \cdot Q_{\text{sw}}}{t_{\text{clk}}} = K \cdot C_L \cdot V_{dd} \cdot f_{\text{clk}} \)

where \( K \) is the switching probability.

- Larger Logic blocks:

  For larger logic, the peak current depends on the gate topology. RAM’s have 2 peaks, 1 for decode, 1 for read/write buffering decode.

  Typically for multistage fast logic, each stage is equalized in delay so that we can often approximate the ensemble peak current by a triangle for each stage.
On Chip Power Distribution

Eq: 1-64 decoder: 0.35 \mu m

Stage 1
6 inverters
1/0.5

Stage 2/3
2-4 decode
2/2 14/7

Stage 4
4/6

6x
6 switch

12x
3 switch

64x
1 switch

* note: only a small number of 2 & 3 will be active.

<table>
<thead>
<tr>
<th>STG</th>
<th>N</th>
<th>S</th>
<th>(L_L)</th>
<th>(C_T)</th>
<th>(C_Q)</th>
<th>(t_r)</th>
<th>(I_{pk})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6</td>
<td>6</td>
<td>18f</td>
<td>108f</td>
<td>0</td>
<td>153p</td>
<td>1.9</td>
</tr>
<tr>
<td>2</td>
<td>12</td>
<td>3</td>
<td>46f</td>
<td>138f</td>
<td>414</td>
<td>201p</td>
<td>1.9</td>
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<tr>
<td>3</td>
<td>12</td>
<td>3</td>
<td>350f</td>
<td>1050f</td>
<td>3150</td>
<td>218p</td>
<td>13.4</td>
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<tr>
<td>4</td>
<td>64</td>
<td>1</td>
<td>100f</td>
<td>100f</td>
<td>6300</td>
<td>217p</td>
<td>1.3</td>
</tr>
</tbody>
</table>

\(C_Q\) is "Quiest" load, those that didn’t switch...
On Chip Power Distribution

* Random Logic Case

Eq: \( N_d = 50,000 \text{ gates} \quad C_L = 100 \text{fF/gate (0.35m)} \)

\( d = 10 \text{ levels, assume } 2K_s \text{ switch each cycle} \)

\((K_s \text{ switch in each direction...})\)

\( N_s = K_s \cdot N_G \text{ in one direction, equalize delay/stage} \)

Triangular stage peak as before:

\[ N_i = \text{number of switching in stage } i = \begin{cases} \frac{4N_{si}}{d(d+2)} & \text{if } i \leq \frac{d}{2} \\ \frac{4N_{si}(d-i)}{d(d+2)} & \text{if } i \geq \frac{d}{2} \end{cases} \]

\( I_i = \text{current in stage } i = \frac{N_i C_L V_{cc}}{t_r} \)

So for our example: \( K_s = 0.25 \quad N_s = 12,500 \)

\( N_i = 2,083 \quad \Rightarrow \quad I_p \approx 2.9A \)

for \( t_{ck} = S_n S \quad I_{Au} = 624mA \)

* Note: we must assume worst case pattern in estimate of \( K_s \) for our design! \( \Rightarrow \) else will “work” sporadically!
On Chip IR Drop

Assume that the power grid is a hierarchy of wires with essentially zero resistance at the periphery:

Assuming periphery has near zero resistance (pods)

Resistive metal layer is constant: \( R = 0.04 \Omega / \mu m \) A
Via = 1Ω (0.35μm)
On Chip IR Drop

Assume metal/via overlaps gates.

\[ R_i = \frac{L_i}{W_i} \cdot r \cdot \frac{1}{2N} \]

\(N\) segments

\[ A_i = \frac{L_i W_i}{k_i} \cdot \frac{1}{N} \]

\(k_i\) = fraction of metal level devoted to power of 1 side:

Eg:

\[ L_p = 15\,\text{mm} \quad K_p = 0.375 = \left(\frac{30}{80}\right) \]

\[ W_p = 30\,\mu\text{m} \quad \Rightarrow \quad N = 187 \]

pitch = 80\,mm \quad \quad \quad \quad A_p = 1.2\,\text{mm}^2

(note: \(A_p\) counts area for \(N\) = # of pairs of \(N, P\))

* Peak Current Drawn by a segment \(\Rightarrow\) Peak current of supplied area.

@ 0.35\,\mu\text{m} : 4 \, K \, \text{gates/(\mu)m}^2\quad K_{sw} = 0.25 \quad \text{we get} \sim 0.26\,A / \text{mm}^2 = J_{pk} \quad \text{and}

\[ J_{avg} = 56\,mA / \text{mm}^2 \]

\[ \Rightarrow \text{Peak/segment} = J_{RR} \cdot A_1 = \frac{0.31A}{N} \]

Each Segment has current = sum of all lower sources

if we assume that \(K_p\) = width/pitch ratio is constant for all levels hierarchy:

i.e., Aspect ratios of each segment is same \(\Rightarrow\)

\[ \Rightarrow \text{all Resistors are equal.} \]
On Chip IR Drop

\[ V_1 = R \cdot J_{RK} \cdot A_1 \]  
(voltage drop)

\[ V_2 = V_1 + R \cdot J_{pk} \cdot A_2 \]

\[ V_i = \sum_{j=1}^{i} R \cdot J_{pk} \cdot A_j = \sum_{j=1}^{i} J_{pk} \cdot \frac{L_j}{W_i} \cdot \frac{r}{2N} \cdot \frac{L_i W_j}{K_i N} \]

\[ = \sum_{j=1}^{i} J_{RR} \cdot \frac{L_j^2 \cdot r}{2N^2 K} \]

\[ \text{as segments } \Rightarrow \infty \]

\[ V_{drop} = \sum_{j=1}^{N/2} J_{pk} \cdot \frac{L_j^2 \cdot r}{2N^2 K} \]

\[ V_{drop} = \int_{0}^{r} \frac{J_{pk} \cdot r \cdot x}{kp} \, dx = \frac{J_{pk} \cdot L^2}{8kp} \]

So for 0.35\( \mu m \Rightarrow J_p = 0.31A / \text{mm}^2 \) \( r_D = 0.04 \) \( L = 15mm \) \( k = \frac{3}{8} \) \( V_{drop} = 0.3V \)

\[ \Rightarrow \text{Total Drop} = [0.6V] \]

\textbf{note:} only can reduce if use thicker wire or more of layer.

* Thicker top level wire \( \Rightarrow R_j \rightarrow \text{reduced.} \)

* Chip pods across area of dil. \( \Rightarrow \) use wire in p.c. board.

* On-Chip bypass
On Chip IR Drop

Metal Migration:

Worry sets in @ $1mA/mm^2 = (10^9 A/m^2)$

so average current must be distributed on sufficient metal

\[
N_{\text{segs}} = \frac{L}{N} = \frac{W}{K}
\]

\[
\frac{K \cdot L}{N} = W
\]

Current/segment = \(J_{AV} \cdot L \cdot \frac{L}{N} = J_{avg} \cdot \frac{L^2}{N}\)

Area of wire ⇒ \(H = \frac{K \cdot L}{N}\)

⇒ \(\frac{1}{2}\) current for each side ⇒ current/area = \(\frac{J_{AV} \cdot L^2}{2N} \cdot \frac{N}{HKL}\)

\[
\frac{10^3}{mm^3} \geq \frac{J_{AV} \cdot L}{2Hk} \Rightarrow K \geq \frac{J_{AV} \cdot L}{2H} \cdot 10^{-3} (mm)
\]

Eq: \(K \leq 0.45 @ \text{example.}\)
<table>
<thead>
<tr>
<th>Parameter</th>
<th>0.25(\mu m)</th>
<th>0.18(\mu m)</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Simulation</td>
<td>Our Method</td>
</tr>
<tr>
<td>(W_p/W_n) ((\mu m))</td>
<td>(C_L) ((\text{ff}))</td>
<td>(t_R) ((\text{ps}))</td>
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<td>50</td>
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<tr>
<td>10/10</td>
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<td>100</td>
</tr>
</tbody>
</table>

Table 1: Validation of expressions for incremental buffer delay and slope changes

\[
\Delta t_{PHL} = K_1 \cdot \Delta V_{com} - K_2 \cdot \Delta V_{diff}
\]

\[
= K_1 (\Delta V_{dd} + \Delta V_{ss}) - K_2 (\Delta V_{dd} - \Delta V_{ss})
\]

\[
K_1 \equiv \frac{t_R}{2 \cdot V_{dd}(1 + \alpha)} + \frac{C_L}{2 \cdot \Delta V_{dd}},
\]

\[
K_2 \equiv \frac{t_R}{2 \cdot V_{dd}(1 + \alpha)} - \frac{C_L}{2 \cdot \Delta V_{dd}}.
\]

\(K_1 > K_2\) for most techologies

\(t_{dd} = \text{Set amount} \cdot U_{dd} = U_{gs} = V_{dd}\)

\(\alpha = \text{velocity SAT index}: \alpha = (1 - 1.2) \cdot \text{typical cmos}\)