Lab2 : RC Dominated Wires and Models

Due Wednesday Feb. 6 (1 week)

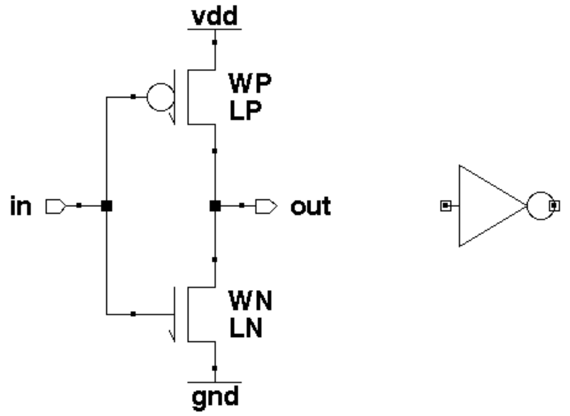

Figure 1. Inverter schematic

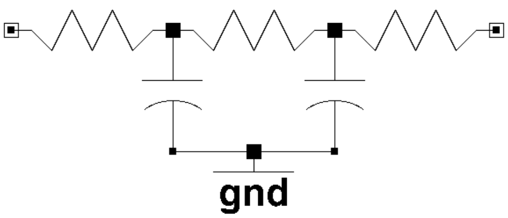

Figure 2. RC wire model

SETTING UP AN INVERTER

In this lab we will transition from using step voltage sources to using an inverter to drive signals. The inverter gives us a more realistic signal and thus better results. To refresh your memory, Fig. 1 has a schematic for an inverter. The transistor lengths should correspond to the minimum drawn gate length for the process (0.18um in this case). Use 4um for the n-channel width and 9um for that of the p-channel side. The rest of the lab will require you to know something about this inverter so the next step is to characterize it. A spice transistor model for 0.18um is available on the web site. Please start this lab early – it is easy to make an incorrect setup and not be able to run the simulations. Starting early allows you to get help if you need it before it is too late.

To characterize the inverter we need to determine its input equivalent capacitance, output capacitance, and output resistance. (The output resistance is for use in a conventional Elmore-delay model). It is important to remember that all these values are nonlinear so we need to be careful to get meaningful data. In this lab, we are interested in the large signal behavior of these devices. Determine the average values for the input capacitance, output capacitance, and output resistance for a inverter in 180nm technology over the 3 following cases: 0->50% rising edge, 100%->50% falling edge and 20%->80% full swing. (Remember that Vdd is 1.8V for this technology). For example, to find the effective input capacitance, remember that $Q = CV$ and here know $\triangle V$, and can simulate to find $\triangle Q$ by choosing a suitable current source (or even a resistor) and charging the inverter over the desired swing, measuring the rise/fall times. Similarly, the output resistance can be found by charging a known capacitance load, measuring the rise/fall time over the appropriate voltage swing and determining the size of resistor which would have equivalent delay times. Finally, if you choose a few sizes of output load capacitor, you can determine the output parasitic capacitance by extrapolating the output delay for zero additional capacitance loading. It is best to choose loads which are comparable to those you are driving in your experiments... 2mm of wire will have (ballpark) 400fF of capacitive load.

EXPERIMENT 1: RC VS. LRC

The previous lab dealt with modeling a wire as a set of lumped LRC segments. For low resistance wires, such as the PCB trace in the previous lab, the LC (transmission line) effects dominated. When using a very lossy line, on other hand, the resistance dominated the behavior. Redo Experiment 4 from Lab 1 with the wire 10mm long this time. Compare the rise time of the signal at 5 equally spaced places along the wire (every 2.5mm). Try this experiment again with the inductors removed from you model. What is different this time? Now collapse the model into one that has 2 capacitors and three resistors as shown in Fig. 2 . Choose the resistors and capacitors so that the total capacitance is equal to the wire-segment that it replaces. (This is called a pi-model because of the circuit topology – it might be instructive to try 1/4,1/2,1/4 for the resistor distribution as well as 1/3, 1/3, 1/3). Measure the output of this condensed (fewer component) model as compared to the other two models. What has changed? By how much? How does the delay of this simple model compare to what Elmore delay predicts? (The rationale for building a simplified model is to allow simpler analysis– which can lead to improved understanding and optimization).

EXPERIMENT 2: ELMORE DELAY ON A TREE

Now we are going to model an inverter driving a fan-out of 3 through some fairly long interconnect. We are going to continue using our global wire cross section from before. Create a RC model for 2mm of this global wire and use it to model the circuit shown in Fig. 3 . How do the delays to each

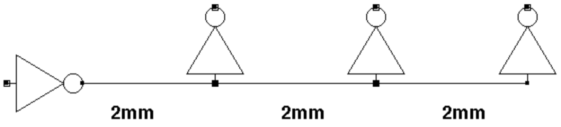

Figure 3. Multiple taps on a line

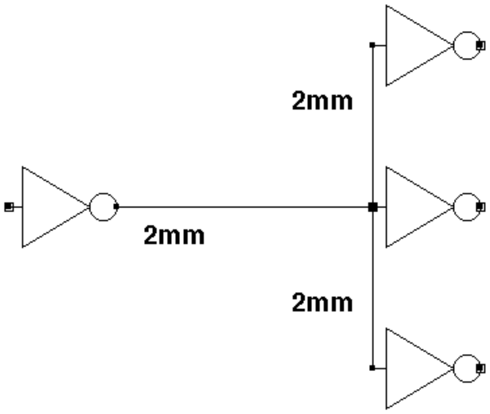

Figure 4. Inverters in a tree configuration

inverter compare to your Elmore delay calculations? Lets say you get crafty with your layout, and decide to layout those inverters in a tree instead of a line. How does the behavior of the circuit shown in Fig.4 compare to the behavior of the circuit in Fig.3? The total amount of wire is the same, but is the rise time at the output of the driving inverter the same? Why? Is this consistent with theory? In general, when simulating CMOS designs, you measure delay from the 50% point of the input to the 50% point of the output swing. This is done since the typical CMOS gate (an inverter) has its maximum gain (gate threshold) at about Vdd/2, although this can be changed by altering the ratio of n and p channel widths. When trying to find estimates of in-circuit delays, be careful to limit the input current and rise-time to reasonable values and to add suitable loads on the output. In the case above, you can drive the inverter with a 100pS rise-time signal, but another small inverter driving the input will give a more realistic result. (This issue is crucial for characterizing complex CMOS gate circuits... as we shall explore later.)