

Lab 1: Long Wires

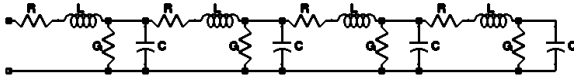


Figure 1. RLCG model

BACKGROUND

Long wires are a major challenge for VLSI designers. Not only are there issues of signal integrity, but there are also difficulties with delay and power consumption. All of these interconnect issues become more prevalent with higher operating speeds. An additional complication in the on-chip realm is the higher operating speed and the small size of on-chip wire, which leads to high loss. As a VLSI designer you need to be familiar with these effects. Transmission lines, as these long wires are sometimes referred to, can easily be modeled with an incremental RLCG (also known as "T") model as shown in fig 1. Luckily for us the dielectrics we use are, in general, not that conductive so we can ignore C for now. The trick to simulating the model correctly is dividing the wire into enough segments that the lumped approximation holds.

EXPERIMENT 1

To kickoff this lab the goal of the first experiment is to determine how small the lumped segments have to be. For this experiment we are working with a PCB trace. This trace is in 1oz copper, 15 mils wide. The trace is on the surface a 4 layer .032 inch thick PCB with a ground plane on each of the internal layers. The trace runs for 6 inches on the PCB. The dielectric constant for the board is 4.2. Use the wire over ground plane calculation found on the back cover of the textbook to figure out the inductance, resistance and capacitance for this wire. Drive this wire with a 0V to 5V rising edge that takes 250ps to swing. To generate more realistic results use a RC low pass filter to kill off some of the higher frequency artifacts. Choose your R and C to give a corner frequency somewhere between 2 and 20 GHz and your R is close to the parasitic impedance of the line. Run this experiment with the lumped segments representing 2cm, 1cm, .5 cm and .25cm and determine the coarsest distance that still gives you delays within 10% of expected.

EXPERIMENT 2

Using the same setup as above, apply a termination resistor to the formally open line and document the results. Short the far end and re-run the test, also documenting the results. Use the resolution that you determined best from the first experiment.

EXPERIMENT 3

Using the PCB setup again simulate what would happen if the wire was routed through a 1nH via 3 inches from the source end. Leave the far end of the wire open. Repeat the test replacing the via with a pad that is 4mm x 2mm. Is the result what you expected?

EXPERIMENT 4

Now let's try simulating on-chip. On-chip signals run much faster than off-chip. The rise time we are going to use is 25ps instead of 250ps. Adjust the low pass filter accordingly. The wire is now 5mm long and on the redistribution layer of a .18u chip. This wire is 1.25u thick, 7u above the substrate, and .9u wide. Because .18 is available in both Al and Cu processes, it is important to remind you that we are using copper. Instead of looking at just the ends of the wire for this experiment, make sure to note the behavior of the wire at 1mm intervals. Because this rise time is approximately 10 times faster than the signal PCB trace we looked at, make sure that you divide the trace into segments 10 times shorter than you chose to use for the PCB test.

WRITEUP

The writeup process should be fairly straight forward. You need to present your findings in a clear and concise manner. Include data tables that contain your findings as well as a few diagrams and signal plots that illustrate the points that you are making. Email the TA the spice deck(s) [* .sp] and header file(s) [* .h] that you used to run these experiments. The files MUST tar'd and compressed. Both the tar file and the email should contain your name and the subject line should mention this class. To generate the tar file from the command line execute `tar -cjvf yourname.tar file1.sp file1.h file2.sp file2.h [...]`

TA CONTACT INFO

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