

ECE 124d

Homework 6

Due: Wed Feb. 27,2008

Reading: DSE chapter 5 (skip 5.2):

- a. inductive power noise
- b. logic power profile
- c. on-chip bypass
- d. symbiotic bypass

Read “Decoupling References” on line

Problems: p. 256, 5.1 (check your model with spice), 5.2, 5.11a, 5.12, 5.13, 5.15

7. Consider a small processor with a 2.5V, 32-bit communication bus operating at 200MHz (1.6nS rise and fall times).

- a. If this bus is driving 50Ω lines on a PC-board, what is the worst case dI/dt if all lines switch at once?
- b. Assuming that the power to drive the board comes from off chip, what is the maximum allowable inductance of the power and ground supplies to the chip to limit the voltage drop and ground bounce to .25V? How many power/ground bumps will this require at 1nH/bump?