

ECE 124d/256c

Homework 5

Due: Wed Feb 20, 2008

Reading: Finish DSE Chapter 4

1. Design a schematic and stick layout for the following cmos complex gates:

a. $f = \overline{ab+ac+ad+bc+bd+cd}$ where arrival order is: a, b, c, d

b. $f = ad+ace+be+dcb$ where arrival is b, (a,c,e), and finally d. (note: can be done in 10 transistors).

2. Do problem 4a using CPL gates.

DSE p. 216 Problems 4-2, 4-3, 4-5