

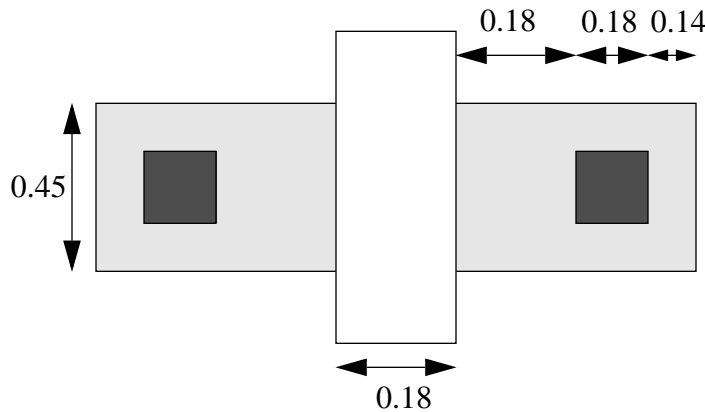
ECE 124d/256c

Homework 4

Due: Wed Feb 13, 2008

Reading: DSE Chapter 4 to 4.3.3

1. For a transistor with the geometry below, calculate values for the parasitic capacitances and resistances as follows: C_{gdo} , C_{db} , C_g , C_d (sidewall), R_s , R_d . Dark color is contact metal, light color is diffusion, white is poly (gate). This size corresponds to a minimum size transistor in your 0.18 μm technology. Find the parasitics above for 2x, 5x, and 10x this width..

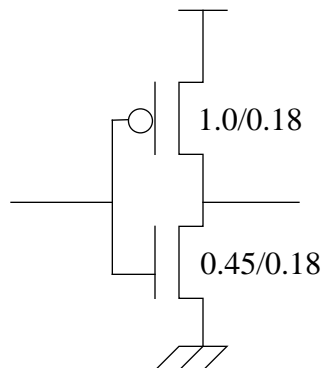


All measurements are in microns, please assume the following process parameters:

n-chan: $\phi_b=0.8$, $V_t=0.5\text{v}$, $k_p=1.8\text{e-}4\text{A/V}^2$, $V_d(\text{sat})=0.4$, $C_j=1\text{fF}/\mu\text{m}^2$, $m_j=0.37$, $C_{j\text{sw}}=0.24\text{fF}/\mu\text{m}$, $m_{j\text{sw}}=0.15$, $\text{tox}=4\text{nm}$, $C_{gdo}=0.8\text{f}/\mu\text{m}$, $\text{rsh} = 7/\text{sq}$

p-chan: $\phi_b=0.84$, $V_t=-0.5\text{v}$, $k_p=-3.6\text{e-}5\text{A/V}^2$, $V_d(\text{sat})=-1.5$, $C_j=1.2\text{fF}/\mu\text{m}^2$, $m_j=0.41$, $C_{j\text{sw}}=0.19\text{fF}/\mu\text{m}$, $m_{j\text{sw}}=0.35$, $\text{tox}=4\text{nm}$, $C_{gdo}=0.65\text{f}/\mu\text{m}$, $\text{rsh} = 7/\text{sq}$

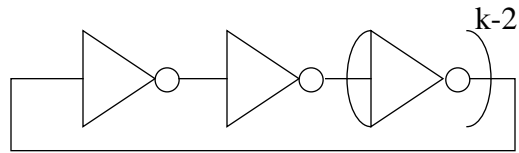
2. Find the propagation delay time for the inverter below.



Assume that V_{dd} is 1.8V and use the electrical parameters from above. Ignore miller feedthrough, but add a linear capacitive output load equivalent to the input load of this inverter. Do not omit the drain junction and sidewall capacitances. Find both rise and fall times for step inputs. For this sizing, what is the inverter threshold (i.e. the input voltage where the output is at $0.9 = V_{dd}/2$)? De-

termine the noise margins by finding the input voltages for which the output slope is -1.

3. Consider the simple CMOS inverter oscillator shown below:



Using the model above for delay through the inverter, estimate the frequency of output f_0 and power dissipation as a function of k . Note: k is odd and should be greater than 5... can you describe (qualitatively) why there is a minimum k ? What happens to a single inverter with its output tied to its input?

Finally, as the power supply voltage is decreased, the frequency of operation should fall. Instead of working too hard, look at the voltage dependent parts of the previous analysis and estimate the frequency dependence on power supply for 1.5 to 2.0 volts. How does the power dissipation scale with V_{dd} over the same range?