ECE 124d/256c
Homework 3

Due: Wed Feb 6, 2008.

Reading: Buffer Paper (on line), Rabaey if desired.

Problems:(Note, these problems are a bit deeper than previous ones -- start earlier to size them up and describe any simplifying assumptions you make.)

1. The repeater optimization proposed by Bakoglu was based on a simple model of a driver in which the output capacitance of the driver is ignored. If the output capacitance is proportional to the driver size e.g. Cout = α W for a given driver width, find a new optimal delay, size and spacing rule.

2. In the buffer paper it is noted that inverter pairs seem to have better jitter behavior than do simple inverters. On the other hand, they are slower. Quantify the difference in performance by finding time-optimal solutions for driver sizing and spacing as follows:
a. assuming minimum length, let the width of the first and second buffers be a and b respectively. Find an expression for the total (Elmore) delay given a,b, spacing and the wire parameters. Derive this model by characterizing a 0.18um inverter designed to have nearly equal rise and fall delays at a few sizes (represented by the parameter 'a' the size ratio to a 'small' 0.18 inverter -- start with 1x equivalent to 0.4um n-channel and 0.9um p-channel widths). Retain this model in your notes-- you will build additional models for .13, 0.045 and other sizes later. {Note that you could do an even better job by allowing the ratio of n to p to change in the two inverters as long as the total delay for the buffer is the same for rising and falling transitions. You need not do this for this assignment -- but the results might surprise you.}

b. Jointly minimize the total delay treating a, b, spacing as independent variables, neglect driver-output capacitance. (you may wish to review the Method of Lagrange Multipliers)

c. Validate your expressions by spice simulation. Use the 0.18um technology and show what choce of effective driver resistance you used. How big of an issue are the short channel effects?

3. Calculate the proper CMOS driver size to source terminate a center driven 90 ohm transmission line with open termination at its ends. Assume that the effective channel resistance for a W=L n-channel is 12k ohms nad a p-channel driver is 40k ohms. If the driver is tri-state (both drivers off) will the line be terminated?

4. For a 30pS rise time, 3V driver sized to 450 ohms driving a 50 ohm, 5 cm, e0=3.5 line, terminated with a pure 10pF capacitor -- plot the potential at the driver output for the first 4 bounces of the wave. To estimate the potential at the capacitor, assume it is charging at the rate of the current flow into it after the wave has passed, until the next wave comes.