

Lab 2A: Gate-Property Extraction and Design for 0.18 μm Devices

Have this done in 1 week! Part B will be handed out next week.

Part 1:

In this lab you extract properties of several gates. These properties include rise times, fall times, noise margins, and power consumption. The first gate is a 2-input static CMOS NAND gate. Note that you should use a buffer to drive the input signals for any transient analysis, since a simple pulse with a rise time does not accurately reflect the input gate capacitance of the gate under test. Also, a buffer should be placed on the output during transient analysis for accurate characterization. For all buffers in this first part assume an inverter with $w_p = 1.84 \mu\text{m}$, and $w_n = 0.92 \mu\text{m}$.

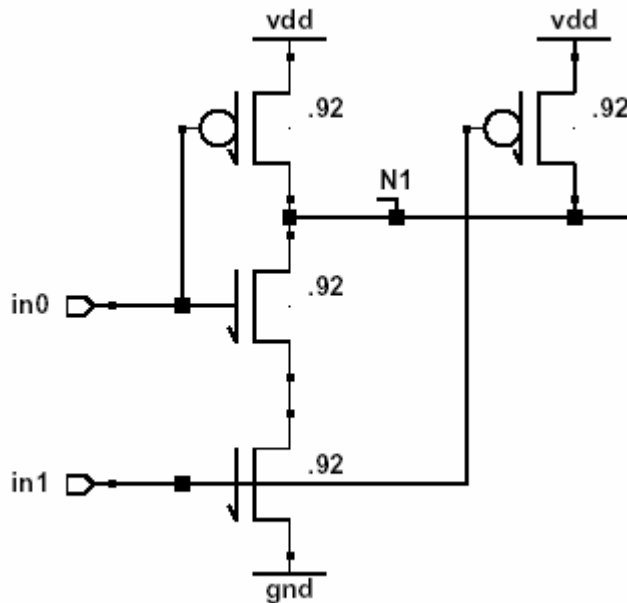


Figure1: Two-input NAND gate. The widths (in μm) are shown. Assume minimum transistor lengths.

First, plot V_{out} of the NAND gate as a function of V_{in} . Since there is two inputs do this for both cases, assuming that the untested input is at V_{dd} . From this plot extract the transfer V_{ol} , V_{oh} , V_{il} , and V_{ih} . You should be able to find definitions for these values in any text on digital integrated design.

Next, extract the propagation delays for all possible single-switching event input combinations (there are four useful transitions).

For each of these four cases plot both the instantaneous power, and also the integral power of the gate. Make sure to include the switching power of the input and output buffers in this analysis also.

Part 2:

Complimentary pass transistor logic (CPL) is a logic family that offers improved performance over conventional static CMOS for many types of gates. It is based on conventional pass transistor logic. Each gate is designed in such a manner that both an output and its compliment are available. The general form of an XOR/XNOR gate is shown below. (All CPL gates have this topology, only the values of the inputs are changed for different functions).

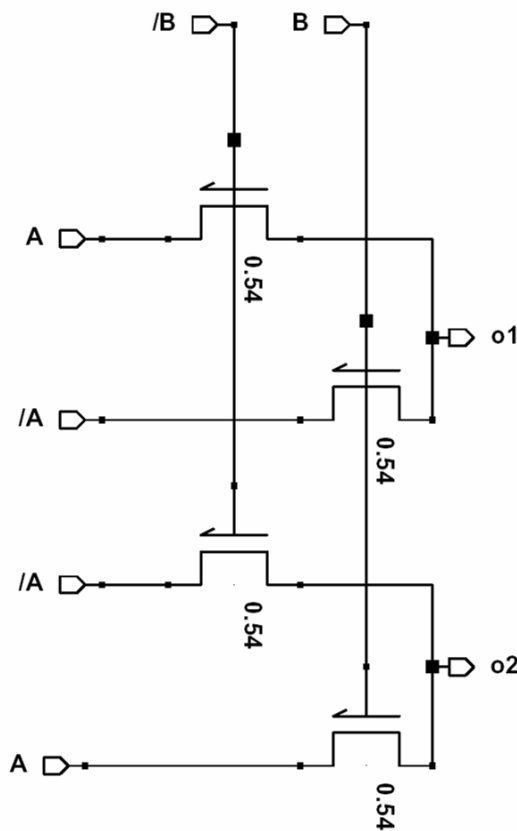


Figure2: Two-input CPL XOR/XNOR gate. The widths (in μm) are shown. Assume minimum transistor lengths.

Note which output is XOR, and which is XNOR.

Extract the same properties for this gate that you did for the static cmos gate in part 1 (V_{ol} , V_{oh} , V_{il} , V_{ih} , propagation delay, and power consumption). For the transient analysis assume that all of the input/output buffers are inverters with $w_p=0.54\mu\text{m}$, and $w_n=1.08\mu\text{m}$. Note the important transitions for extracting switching characteristics. Also,

make sure that you extract two sets of noise margins (One at the output of the gate, and the other at the output of the inverter)

How can you reduce power consumption when the output is tied to an inverter?
Change your circuit so that it does not consume static power, and plot the integral power of the whole system.

What happens if the compliment of a signal arrives later than the signal?

This CPL gate can easily be converted into a NAND gate by simply changing the order of inputs, and thus the performance does not vary much between the XOR/XNOR CPL gate, and the AND/NAND CPL gate. Compare the gates from part 2 and part 1. Analyze the differences in terms of noise, power and speed.

Part 3:

Use complimentary pass transistor logic to design a full adder. Use the propagation delay as your measure of performance. Your circuit should have very little static power dissipation, and the output should be buffered. Beware of sneak paths in the logic, but optimize the performance subject to low static power.

For all parts assume a power supply of 1.8 V, and an input signal rise time of 25ps.