

Lab 4: Clock Network Design

Introduction:

In class you have learned about clocking, and its implications on timing for an integrated circuit. In this lab you will design a clock distribution network with the objective to maximize the available clock speed, and also to minimize the total power.

Lab:

Several options are discussed in the text for designing clock distribution (H-trees, mesh distribution, etc.). Your job in this lab is to design a clock distribution network to satisfy an integrated circuit that is 1 cm^2 with approximately $2 \cdot 10^5$ uniformly distributed flip-flop's. Each one of these FF's has an input capacitance of 6 fF . Note that these FF cells have an input buffer, which lowers the capacitance.

Cost Functions and Constraints:

In designing your network you may design up to three types of buffers (inverters) to drive your circuit (small, medium, and large buffers). These clock buffers should have symmetric rise and fall times to minimize jitter in the distribution tree. In your design, you must also specify the layout geometries of the metal layers. The parasitic values for these elements are given in table 1. Assume that the top-level clock is coming out of a phase locked loop, and that the rise time of the signal out of the PLL is $30 \text{ ps} + 40 \text{ ps}/15 \text{ fF} \cdot C$, where C is the effective capacitance of your first stage of inverters. In addition you are required to deliver a signal with less than 150 ps rise/fall times to each FF.

Assume that the minimum clock period that you can support is $4 \cdot t_s$, where t_s is the total series clock skew. Assume that the skew of a buffered section is simply $2 \cdot t_r$, where t_r is the rise-time at the input of the buffer (Assuming approximately 200 mV of supply noise). Your design must reach 250 MHz at least. Use f / p as the measure of performance of your system, where f is the maximum clock frequency, and p is the total power requirement. Make sure that you state the power requirements, and the maximum clock frequency clearly in your write-up.

Use hspice to aid you in your design, and include the appropriate spice plots in your write-up showing what the appropriate rise, and fall times are at the inputs to your buffer stages. Be smart about your simulations. You don't need to (can't) simulate the whole circuit. For example, if you're careful about load capacitances and power scaling you only need to simulate a path from the root to a leaf flip-flop. Further, to lower the power requirements, you should carefully consider the location of buffers in the network and their size as well as the interconnection widths and connection strategy. If you choose to use different wire lengths to different nodes (e.g. to lower wire usage and power) you must add the estimated skew to the jitter valuation from above. Your goal, once you reach 250 MHz is to minimize the power requirements.

	<i>Area Capacitances (aF/μm^2)</i>	<i>Fringe Capacitances (aF/μm)</i>	<i>Sheet Resistance (milliohms/square)</i>
Top 2 Metal Layers	37	53	40
All Other Metal Layers	37	53	80

Table 1: Parasitic wire values.