

## Lab 3B: Decoupling Power Supply Networks

### Introduction:

A typical integrated circuit can draw over 60 Amps of current instantaneously (within hundreds of picoseconds). This poses a problem for the designer: How do you feed this much current to your circuit when a typical power supply bandwidth is limited to 50-100 KHz? In this lab you will use decoupling capacitors to solve this problem.

### Lab:

You are given the power supply network in figure 1. Notice that three capacitors do not have values attached to them. These are the capacitors (or capacitor arrays) that you will introduce into the system to overcome power supply noise. The purpose of the capacitor that is closest to the supply is to decouple the physical power supply. The middle capacitor is the lump sum of the capacitors at the board-level off of the package. Finally, the capacitor closest to the output is the package capacitance. For the lab you will have several capacitors to choose from, each having a different price, and different parasitic resistance and inductance. These parasitics are modeled as a resistor and an inductor in series with the decoupling capacitor and come from currently available parts. The model is shown in figure 2.

Use the above models to decouple each stage of the power supply for three waveforms (Given below). Keep track of how many capacitors you use, and the cost of the components (Discussed below). Also, record the worst case deviation of the supply voltage at the integrated circuit. Explicitly report this value as a total of the percent power supply voltage. Also report the number and types of capacitors used for each section, and the total cost. Use  $1 / (V(\%) * \text{cost}(\$))$  as your measure of performance. Make sure you state this value clearly in your report. You must keep the supply deviations within 0.3V of the nominal rail as an absolute max. Note that you may have to use more than one capacitor at each point (in parallel) and possibly more than one type at each point.

### Input waveforms:

Model the integrated circuit current-draw as a sum of 3 current sources shown below. (Current sources add in parallel!) Decouple the system rails over the full range of frequencies. You may wish to solve the decoupling for each source independently to reduce the spice simulation time, but verify your design with all sources in parallel and a run sufficiently long enough to cover the longest period sources. Ensure that your circuit is decoupled for at least 10 waveform periods.

Waveform 1: A triangle current pulse with rise time = fall time = 130 ps and a peak current of 45 Amps with period of 3 ns.

Waveform 2: A square current pulse with rise time = fall time = 150 ns, length of 160ns and a peak current of 7 Amps with period of 500 ns.

Waveform 3: A square current pulse with rise time = fall time = 2  $\mu$ s, a length of 3 $\mu$ S and a peak current of 6 Amps with period of 10  $\mu$ s.

Capacitors:

You will be allowed to use nine different values of capacitors (figure 3). Each capacitor's cost depends on the type of the package (figure 4) with the exception of tantalum capacitors. You can choose between four types of packages. The more expensive packages have smaller parasitic inductances.

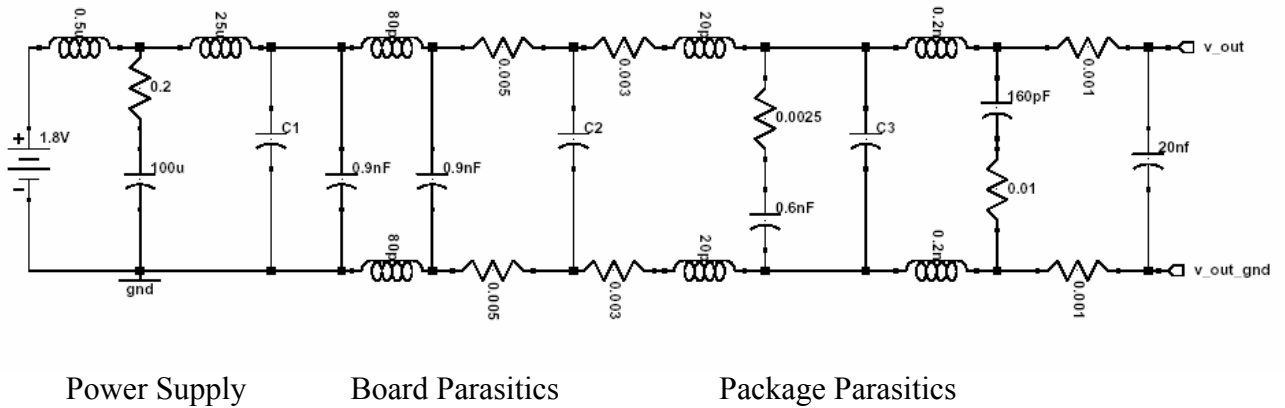


Figure 1: Power Network Model (Current source is attached between v\_out and v\_out\_gnd)

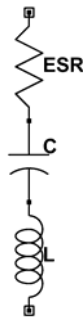


Figure 2: Capacitor model with parasitics

Capacitance Value	Capacitor Type	ESR (ohms)	Cost (\$)	Parasitic inductance
10 pF	NPO	0.01	See Package	See Package
100 pF	NPO	0.01	See Package	See Package
1 nF	NPO	0.01	See Package	See Package
3 nF	X7R	0.5	See Package	See Package
30 nF	X7R	0.5	See Package	See Package
220 nF	X7R	0.5	See Package	See Package
5 uF	Tantalum	0.05	0.9	2 nH
100 uF	Tantalum	0.05	2	3 nH
1500 uF	Tantalum	0.05	5	4 nH

Figure 3: Capacitor types, values inductances, costs.

Package Type	Cost (\$)	Parasitic Inductance
1206	0.2	1.2 nH
612	0.4	170 pH
612IDC	2	60 pH
LICAS	20	26 pH

Figure 4: Package Types, costs, and inductances