

## Lab 3A: Influence of Logic Design on Power Supply Networks

### Introduction:

In Lab 2 you had the chance to optimize two different flip-flops (FF) for power and speed. In this lab you will consider the implications of your design on a power distribution network.

### Part 1:

The beginning of a decoder is shown below. It consists of an input segment latching the input signals (Figure 1) followed by a logical and gate (Figure 2). The circuit that you will use for this lab consists of 4 copies of the input stage driving 16 copies of the logic path wired as a 4-16 decoder.

First, extract the transient current characteristics for the given circuit. Use your flip-flop from part 1 of Lab 2 for the input FF. Use an input vector such that each gate in the logic path switches. Do this with two input vectors such that the output switches from high to low and low to high. You do not need to fully exercise all transitions of this circuit as long as you have a sample of each differing transition.

You may use a clock period of 5 ns (will not matter for analysis). Assume a clock rising edge and an input signal rising edge of 30 ps. Make sure that you take small enough transient steps such that you can get an accurate representation of the waveform. What is the peak current and total charge over the cycle? Now assume that the clock signals into each of the flip-flops are subject to timing skew of 30pS. (Simulate this by making 4 clock sources with differing time offsets). Again measure the peak current and total charge used over a cycle.

Simulate an additional input vector such that only two of the NAND gates switch.

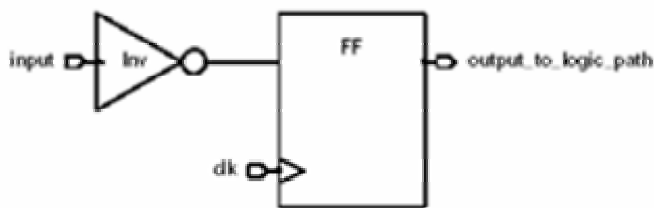


Figure 1: Input structure Use  $w_p=1.84\mu\text{m}$   $w_n=0.92\mu\text{m}$  for the inverter.

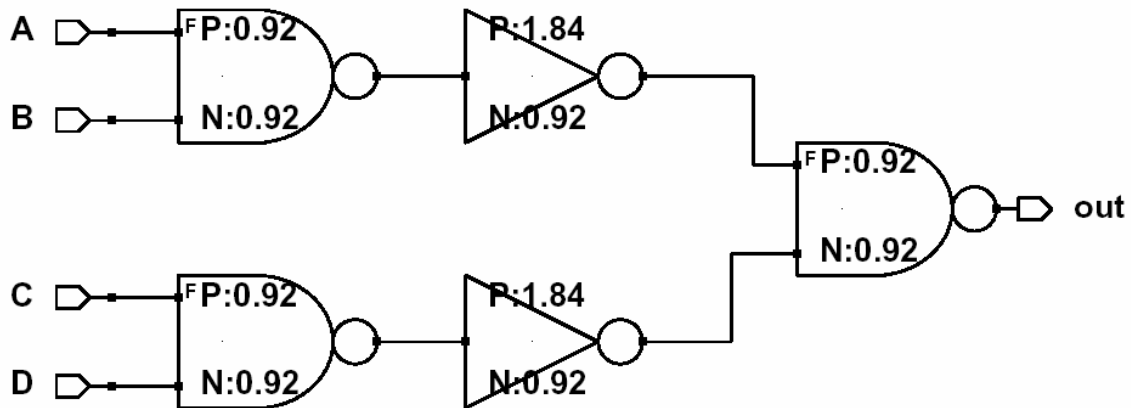


Figure 2: Logic Path (Widths are given)

Part 2:

Repeat part 1 for the C<sup>2</sup>MOS FF that you designed in lab 2.

Answer the following questions for part 1 and 2:

Assume that 25% of your gates are switching during a clock cycle. If you can supply 8A peak to your integrated circuits, what is the maximum number of similar logic paths that you can support? What is the maximum current slew rate that you will need to supply (in Amps/s) for this number of circuits? What is the required bandwidth of the power distribution network? (Here you need to find the maximum  $dI/dt$  over the current profile. Note the typical triangular shape of the current pulses for CMOS based drive currents—these can be superposed to estimate the peak current in a subsystem. Can you find a simple relation between the propagation time, the gate size and the peak current for the integral charge over a cycle?