

Lab 2B: Latch-Property Extraction and Design for 0.18 μm Devices

Part 1:

In this lab you will design and extract properties of two master-slave flip-flops. The first flip-flop is shown below, and consists of transmission gates driven by simple inverters.

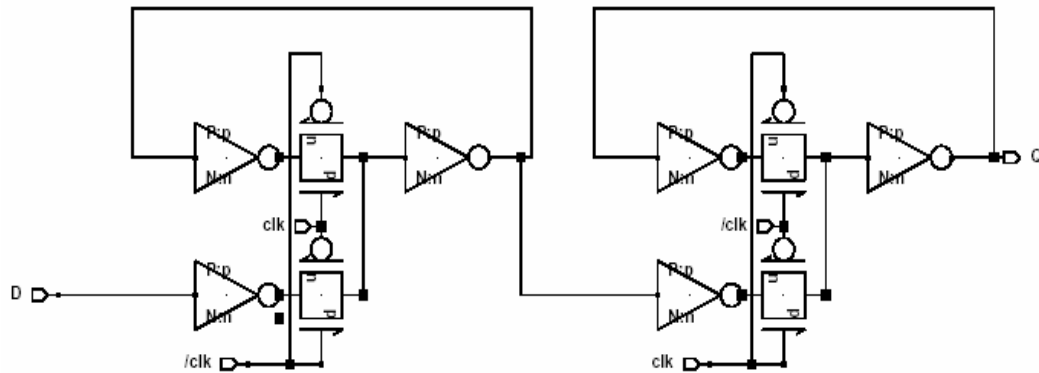


Figure 1: Master-slave flip flops built from pass-transistor multiplexers

Clock to Q time is the measure from the clock edge to a stable output. Size the FF such that the clock to Q time and integral power consumption are minimized. Use $1/(P \cdot t)$ as the measure of performance. Also, note the switching and integral power consumption of the gate for a variety of setup times that approach the minimum. You should also extract the setup and hold time for the circuit. Note: A simple way to extract the setup time is to run two signals with a period that varies by only a tiny time margin. You can then route one signal to your clock, and the other to the data signal, and simply note the difference in the two times when the setup fails. For your measure of performance power assume that the data signal arrives well before the clock. Plot the total power per clock vs. setup time for several iterations of your design. **For the initial characterization generate /clk with an inverter from the clk signal.**

Given the extracted setup and hold times what is the upper limit on clock speed? What is the minimum delay needed between two positively triggered flip-flops?

Assume that you distribute your clock poorly, and that the phases overlap by 70 ps. Re-extract the performance and power consumption.

Part 2:

For this part you will size and test a C²MOS FF. The structure for the circuit is given below.

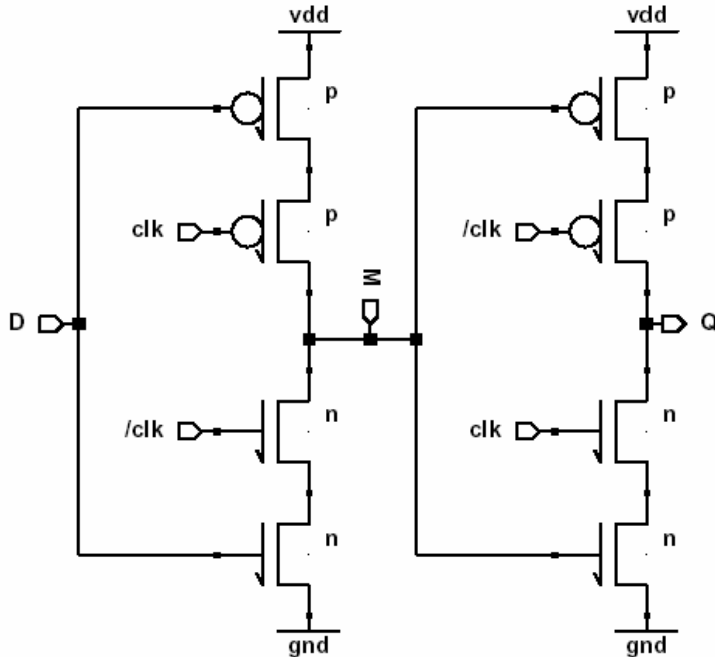


Figure 2: C²MOS flip-flop

Size the transistors to optimize the clock to Q time and power-consumption. Once again, extract the setup time, hold time, instantaneous power, and integral power for all useful switching events. Given the extracted setup and hold times what is the upper limit on clock speed? What is the minimum delay needed between two positively triggered flip-flops? Also, what is the minimum clock speed?

Again, assume that you distribute your clock poorly, and that the phases overlap by 70 ps. Re-extract the performance and power consumption.

What happens to the performance if you assume a parasitic capacitance of 20 fF between the node M and ground.

Comment on the differences in performance, and robustness of both circuits.

Assume a 1.8 V supply, and an input rise time of 25 ps. Remember to use buffers on your inputs and outputs. Assume $w_p = 0.54\mu\text{m}$ and $w_n = 1.08\mu\text{m}$ for the buffers.