Lab #1

Introduction to MAX and HSPICE

Objective

To learn how to lay out VLSI circuits by using *MAX*, and simulate the circuits using *HSPICE*. Students are required to build a ring oscillator circuit and simulate it.

Environment Setup

A startup package which contains initial setup files and scripts is ready to download from the class website (http://bears.ece.ucsb.edu/class/ece124a/). Download the package and extract it by using command:

```
gzip –c –d 124a.tgz | tar xf –
```

This will create a sub-directory named *ece124a* for you. Please change your working directory to *ece124a*. You can do it by using command:

```
cd ece124a
```

From now on, we will assume you are working within *ece124a* directory. Please take a look at the **README** file to see what is included in the package.

For those who haven't used UNIX/LINUX shells before, please copy the file **.cshrc** to **your home directory** by using the following commands:

```
cp .cshrc ~/
source ~/.cshrc
```

.cshrc contains critical information that allows you accessing all the 124a programs. Please note that **.cshrc** is a hidden file and you will not see it with **ls** command unless you type **ls -a**. Also, you only need to run the above commands once.

Using MAX Layout System

Use the following command to bring up *MAX*:

```
max
```

Do the following in the *MAX* design environment:

1. Go to Help->MAX Tutorial and run through the tutorial for information on how to use *MAX*.
2. Build an **inverter** with *fet lengh* = 0.24µ and N/P *fet width* = 2.0µ.
3. Use Tool->Calibre DRC... to check your designwork and fix all reported errors.
4. When you are done building the **inverter**, build a ring oscillator circuit by instantiating 9 inverters in series. Name the circuit as **osc**. There must be odd number of inverters on the ring (why?). Again, use Calibre DRC... to check errors.

WARNING: SAVE YOUR WORK PERIODICALLY TO AVOID DISASTER!!

Running Simulation

Once the layout passes the DRC check, you can use script: **rc_ext** to generate spice netlist of your design. You will find the file named **osc.gds** in your working directory, which is the binary output of your design. Use the following command to generate the spice netlist from the output:

```
rc_ext osc.gds
```

Check *osc.xcalibre_log* for errors. Two files will be created after the process: **netlist.distributed** and **netlist.distributed.pex** Take a look at both files and get familiar with the format. In the future labs, you will have to modify the files to fulfill the simulation requirement.

Next, run the following command to simulate your design:

```
spice_it osc.sp
```

Check *osc.hspice_log* for errors. A waveform file named *osc.tr0* will be created if the simulation is concluded. Use **nst** to view the waveform and do measurements:

```
nst osc.tr0
```

Data Collecting

You need to collect the following data from your design simulation:

- Frequency of your ring oscillators (50% crossing).
- Rise time of the waveforms (20% - 80%).
- Fall time of the waveforms (80% - 20%).
- Redo all the above steps with N *width* = 2μ, P *width* = 5μ.

Designwork To Turn in

- Layout plot of inverter cells.
- Layout plot of ring oscillators.
- Printout of the waveforms.
- Technical report to analyze the results obtained.

10% Extra Credit

Redo the design with different # of inverters in the oscillator and compare the results.

Reference

- Calibre DRC manual (linux): /eci/mentor/ixl_cal_2002.5_16/shared/pkgs/calbr_docs/pdfdocs/calbr_ver_user.pdf
- xCalibre (rc_ext) manual (linux): /eci/mentor/ixl_cal_2002.5_16/shared/pkgs/xcalbr_docs/pdfdocs/xcalbr_user.pdf
- hspice manual: /eci/hspice/2001.2/docs/pdf/hspice.pdf
- nst manual: /eci/mmi/doc/nst/nst_manual/nst_manual.html
- max manual: /eci/mmi/doc/max/max_manual/