

# POWER AND SIGNAL INTEGRITY IMPROVEMENT IN ULTRA HIGH-SPEED CURRENT MODE LOGIC

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## ABSTRACT

Current mode (ECL) logic has long been the option of choice in those applications requiring logic functions at multigigahertz rates. This trend continues despite the obvious very high static power consumption and small signal swing characterizing this logic. In this work we investigate a simple mechanism for Low-Voltage-Swing Logic (LVSL) to greatly reduce the power requirement of a CML logic subsystem while improving the reliability and signal integrity. For the presented circuits operating at 5 GHz, 50% power reduction is achieved while improving the signal integrity.

## 1. INTRODUCTION

High-speed applications such as telecommunications, microwave digital processing, and satellite communications can benefit immensely from an increase in logic function density and a decrease in power consumption. This is especially true for satellite communications. The more functionality that can be placed on a microchip, the lower the overall system cost. This economy of scale and low power is achieved in CMOS at clock frequencies below a gigahertz.

Presently, LSI applications which require operational speeds of 5 GHz or higher are well beyond the domain of CMOS. IBM recently fabricated a CMOS integer processor at 1 GHz [1] and others have reported small circuits such as phase-locked loops operating at 3 GHz [2]. To date, no one has reported LSI CMOS circuits being clocked in excess of 5 GHz. CMOS power dissipation is heavily dependent on the clock frequency. This dynamic power dissipation means that power savings of CMOS is small at multigigahertz rates. The ECL logic family is primarily used at these frequencies, even though ECL has other disadvantages. ECL often uses multiple power supplies which increases system complexity and cost. Also, ECL dissipates much more static power than CMOS, making it impractical for LSI applications. Typically, implementation of a complex (LSI) function in ECL requires splitting the function over several chips so that the power budget of each chip can be kept at a reasonable level. For complex systems, ECL is used only on the front and back ends. The complex functions are implemented in CMOS at demultiplexed clock rates. This, again, increases system complexity and cost. Having a function split into several chips will reduce the overall performance if there is a feedback loop in signalling over several

chips. It also increases overall power since more I/O pads are needed to drive intermediate signals off-chip. The bottom line is that there is no viable power-conserving technology for multigigahertz logic in portable applications although there have been low-power circuits in the lower gigahertz range of 3 GHz or less [3][4][5][6].

An issue inherently connected to power dissipation is thermal management. Higher heat decreases the reliability of the chip. Higher operating temperatures increase thermal noise and reduce noise margins. The large power dissipation in ECL means that chip cooling is a serious concern. Water cooling might be needed for LSI applications. The plumbing and refrigeration unit needed for water cooling increase the system cost. Unlike CMOS, gates cannot always be placed a minimum distance apart. Some ECL gates dissipate such a large amount of power that if these gates are placed too close together, hot spots can develop on the chip. This can be a problem even with water cooling because the thermal conductivity of the substrate may not be adequate to distribute the heat. Placing the gates further apart increases the wire parasitics and requires gates with larger drive capability to maintain the signal integrity. However, gates with larger drive also have a larger power dissipation which, in turn, forces the gates even further apart. This cycle makes many large-scale designs impractical.

To address this problem, we need to analyze where most of the power is being dissipated. Despite the large static power used in CML gates, most of the power is actually being dissipated in long wires and in support of long wires, particularly the clock-distribution network. The emitter followers used to drive long wires have good drive capability but also dissipate a large amount of power. An example of the power budget distribution can be seen with a 40-Gbit/s encoder chip designed and fabricated last year by our group [7]. This chip performs channel encoding for a fiber data network. The operating clock frequency is 5 GHz with new data arriving on both clock edges. The chip has approximately 3800 HBT transistors, dissipates 11.4W total, and is 4mm by 5mm. The chip is large given the small number of transistors to keep the power density reasonably low. Of the total power, 8.22W is due to buffers of various types. Thus, 72% of the total power is dedicated to driving wires instead of performing logic functions. This percentage does not take into account the power dissipation from the pad drivers. If the pad drivers were factored in, the percentage would be closer to 80%.

The power density of the encoder chip is 57 W/cm<sup>2</sup>. This power density requires water cooling for proper operation. The circuit technique we propose in this paper can reduce the power by 50%. If this technique is applied to the encoder then the power density will drop to 28.5 W/cm<sup>2</sup>, thus allowing the chip to be air cooled. In fact, this new power density is in the same range as today's most advanced CMOS chips. The Alpha 21264 microprocessor has a power density of 22.9 W/cm<sup>2</sup> [8] and is air-cooled.

## 2. TECHNICAL DISCUSSION

As the majority of the power dissipation is due to driving long wires, it is obvious that reducing the power of the logic gates would result in minimal improvements in total power reduction. To reduce the power substantially, the buffers driving long wires need to be changed. If the voltage swings can be reduced while maintaining large current swings, then the effect of parasitic capacitance in long wires can be minimized. Further, we can match the drive to the wire impedance, thus improving the signal integrity. Typical high-speed CML already has relatively small voltage swings of 300 mV; If this swing could be dropped to 50 mV while maintaining large current swings, the large parasitic capacitances of long wires will not greatly increase rise and fall times. Thus long wires can be driven with considerably smaller buffers and yield large power savings. If the gates driving long wires dissipate less power, gates can then be placed closer together, thus reducing wire lengths and parasitics. This tighter placement, in turn, allows further reduction in the power of the gates and a large decrease in power dissipation results.

There are different solutions for LVSL and for addressing the high-speed low-power problem in general. Some of these are transistor techniques [9][10][11] while others are circuit techniques [12][13][14][15][16][17][18][19]. The solution proposed in this proposal is a circuit technique called Transimpedance Transconductance Logic (ZGL). A ZGL buffer with differential input and output is shown in Figure 1. Basically, transimpedance amplifiers are added to the differential inputs of a CML gate. Nodes ap and an are the differential inputs to the transimpedance amplifiers which consist of Q1, Q2 and the biasing resistors. Since a transimpedance amplifier translates small current swings to large voltage swings, the internal nodes of a ZGL gate which are not dominated by large interconnect parasitics have the normal voltage swings of ECL gates. The output side of the gate (nodes bp, bn) is a transconductance amplifier which has a current swing proportional to the input voltage swing. This allows long interconnect wires to be driven by gates with a voltage swing as small as 50 mV. The resistors can be adjusted for impedance matching and current drive.

Experiments on the drive properties of ZGL buffers were performed in Hspice. All tests were on circuits running at 5 GHz. The tests on ZGL gates driving long wires were performed with RC and RLC parasitics. The resistance of the wires was estimated to be 20 ohms/mm. The capacitance of the differential wires was estimated to be 80 ff/mm to ground and 68 ff/mm to each other. Finally, the inductance was estimated to be 1.46 nh/mm of self

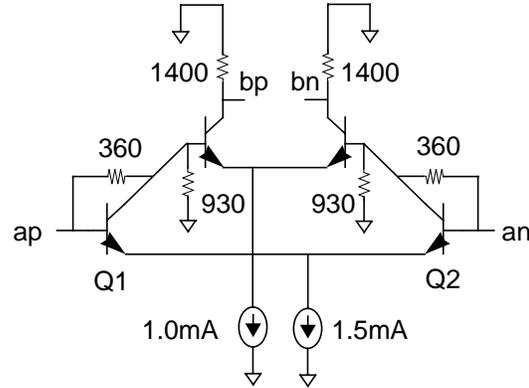


Figure 1. ZGL buffer with differential input(a) and output(b)

inductance and 1.24 nh/mm of mutual inductance. Note that the use of differential interconnect is common with most current mode logic. There are several benefits of differential wires over single-ended wires. The first benefit is that there are fewer gates in the overall design. This is because the complement of every signal is available. The second benefit of differential wires is an improvement of signal integrity. The third benefit is a built-in return-current path for every signal wire. Signals are compared to their complements so shifts in the ground voltage do not affect differential reception. At first, it may seem that routing is more congested and problematic than for the single-ended interconnect common in CMOS. However, as mentioned earlier, the layout of current mode logic is limited by the power density more than by the gate-to-gate interconnect.

A circuit for measuring the parasitic effects on ZGL gates can be seen in Figure 2. This is a series of the ZGL buffers from Figure 1 driving a pair of differential wires 3mm in length. The input for the first buffer is a periodic pulse train. The second buffer is driving the long differential wires. The wire length is modeled with an RLC ladder. The results can be seen in Figure 3. The nodes plotted are the input and output of the second and third buffers. The nodes ap, an and yp, yn are the differential input and output of the second buffer. The nodes y12p, y12n and z0p, z0n are the input and output of the third buffer. The power is the total power of all four gates. These results can be compared to Figure 4 which is a simulation of the same circuit but with ECL emitter followers. There is substantially more ringing in the ECL circuit. This illustrates one of the benefits of ZGL. The low impedance on the input side of the receiver's transimpedance stage matches with the low impedance on the output side of the driver's transconductance

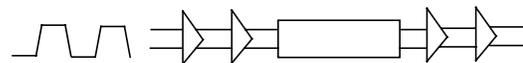


Figure 2. ZGL buffers driving long differential wires

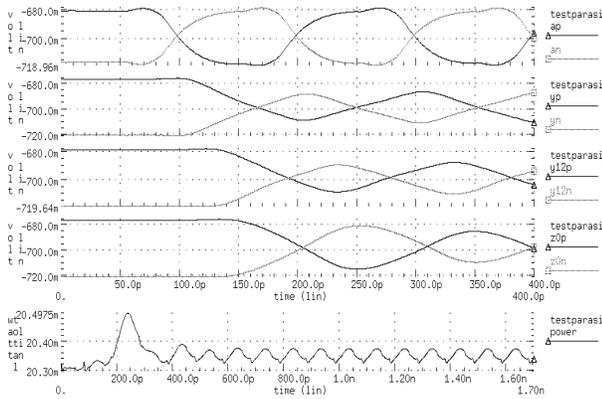


Figure 3. ZGL buffer driving long differential wire

stage. Also, the power dissipation of the ECL circuit is three times larger than the ZGL equivalent.

The power-delay product of ZGL gates is worse than ECL gates if there is no RLC loading on the buffers as can be seen in Figure 5 and Figure 6. These two figures are results of the same circuit in Figure 2, except there is no long wire segment between buffers 2 and 3. That is, the buffers are connected directly to each other. With RLC loading for a long wire as seen in Figure 2 and Figure 3, the power-delay product is markedly better than ECL. As chips get larger, the interconnect delay will dominate the gate delay so the individual gate delay matters less. This dominance in interconnect delay can be seen in the previous examples.

The ability of ZGL buffers to drive clock trees and long wires was put to the test in the aforementioned encoder chip. A major subsystem of the encoder was simulated with all ECL gates and the result was compared with the same subsystem having all the ECL buffers replaced by ZGL buffers. This subsystem is a population counter which counted the number of 1s in a 4-bit input. The original subsystem with all ECL gates dissipated 830mW while the mixed version dissipated 445mW. The mixed version simply had all the ECL clock buffers replaced with ZGL buffers. Both cir-

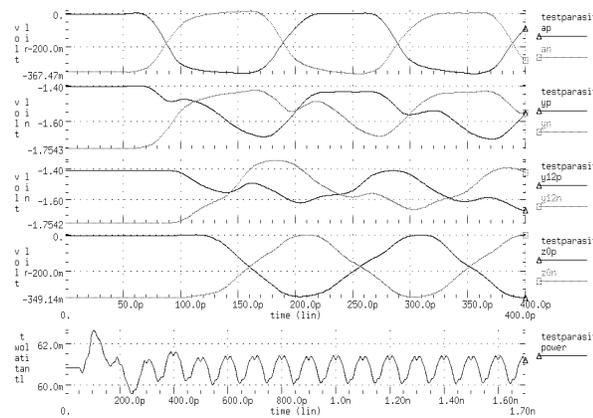


Figure 4. ECL buffer driving long differential wire

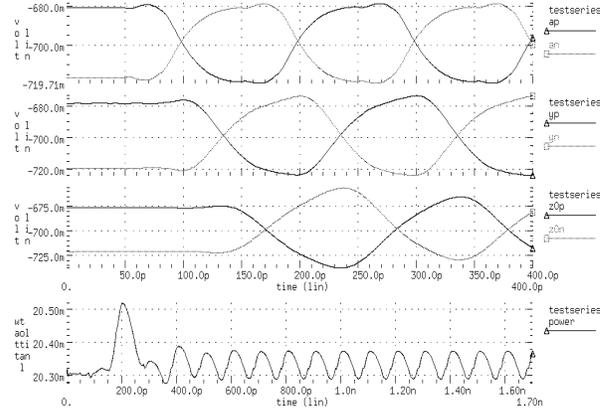


Figure 5. ZGL buffers in series

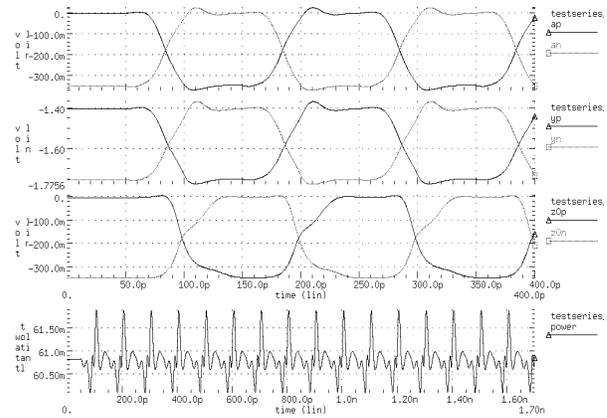


Figure 6. ECL buffers in series

cuits were designed to operate at 5GHz and were simulated at 5 and 6GHz with RLC parasitics, with the parasitic capacitances being extracted from the actual layout. The Hspice outputs (at 6GHz) of the ECL and mixed versions are shown in Figure 7 and Figure 8, respectively. It should be noted that this power saving is obtained with the original placement and parasitics. In reality, the power savings is even greater because the gates can now be placed closer together with the correspondingly lower parasitics.

As seen in Figure 7 and Figure 8, the signals for the mixed version of the population counter are noticeably cleaner than the pure

ECL version. The mixed version is also slightly faster than the ECL version. This improvement in speed and noise is due to the better impedance matching on long wires. Driver sizes in the ECL version were dictated by signal integrity and were very large which, of course, dissipated a great deal of power. The improvement in impedance matching and power-delay product for long wires using ZGL means that the circuit does not have to be over-designed by such a large margin.

### 3. CONCLUSION

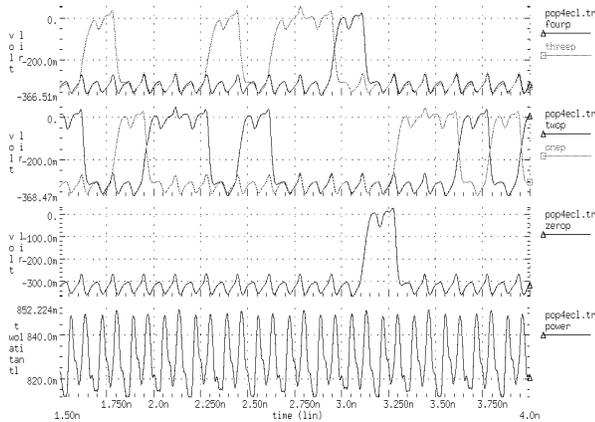


Figure 7. ECL implementation of population counter

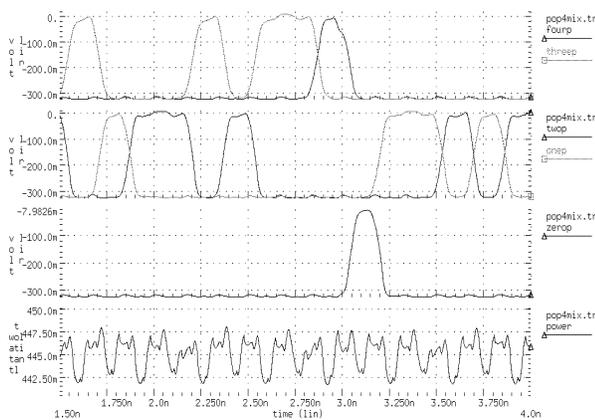


Figure 8. ZGL and ECL implementation of population counter

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