Issues in High-Level Connectivity Synthesis

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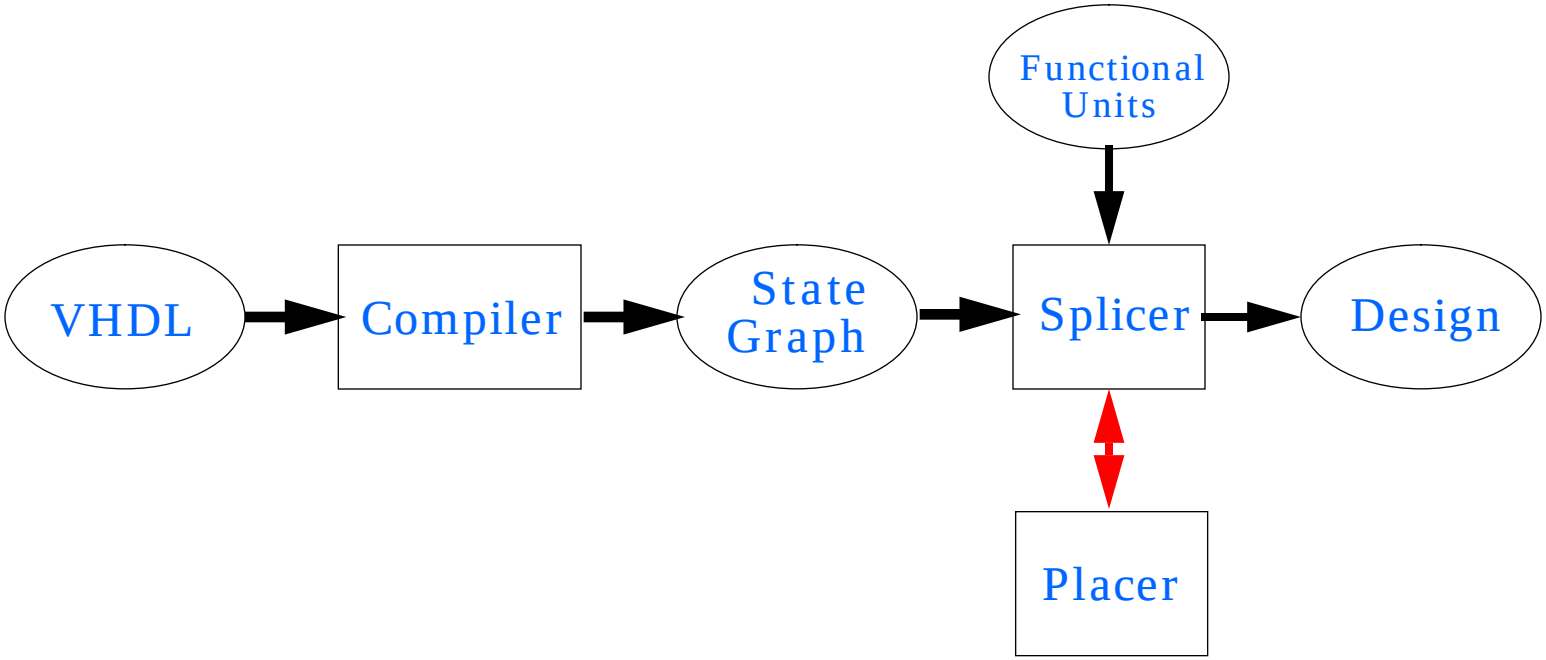
Introduction

- Concurrent Interconnection Synthesis and 1-D Layout Generation
- Multiplexer/Bus Trade-Offs
- Busses, Registers, and Tracks

Related Work

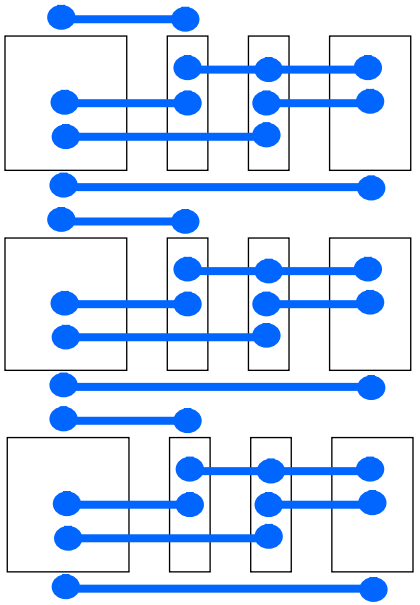
- Hercules, ELF, HAL, LYRA, MAHA, Facet
- PARBUS, CATHEDERAL-II, SPAID, SYCO, BUD

System


Functional Units
VHDL
Compiler
State Graph
Splicer
Design
Placer

Model and Constraints For these Experiments

- 1-D Bit-Sliced Placement Model
- Track Minimization Primary Objective
- Sized Cells
- Busses Used Once per Clock Cycle
- Unidirectional Data Transfers
- Cell Inputs are Not Latched
- Minimum Register Designs

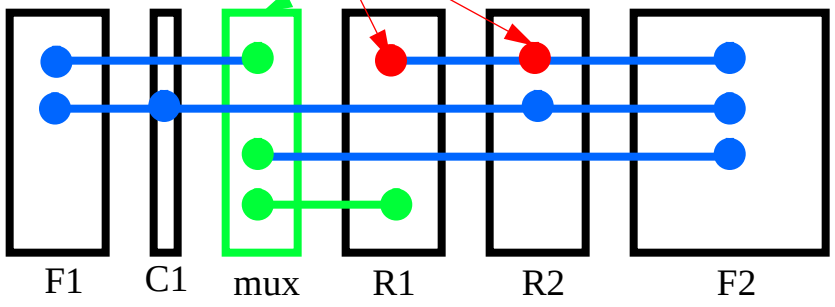


Connectivity to Layout Mapping

C1	R1	R2	F1	F2 (Outputs)						
			X		Bus1				X	
	X	X			Bus2			X		
X		X			Bus3	X	X			
				X	Bus4				X	X
					Inputs:	F1	F2a	F2b	R1	R2

Multiple drives here are bus drivers

Multiple drives here are multiplexers



Busses, Registers, and Tracks

- Number of Tracks Needed In a Design is not Equivalent to Number of Busses
- More Than the Minimal Number of Registers In a Design Can Save Tracks
- What Is The Maximum Number of Tracks Necessary In a Design, If the Number of Registers is not Minimized?

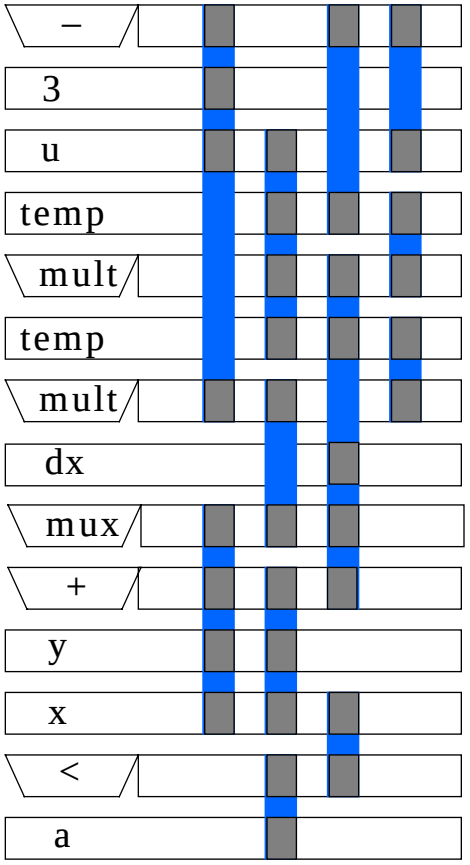
  Lemma:

  An Upper Bound is Number of Simultaneously Active Functional Unit Outputs Plus 2*

*binary operations

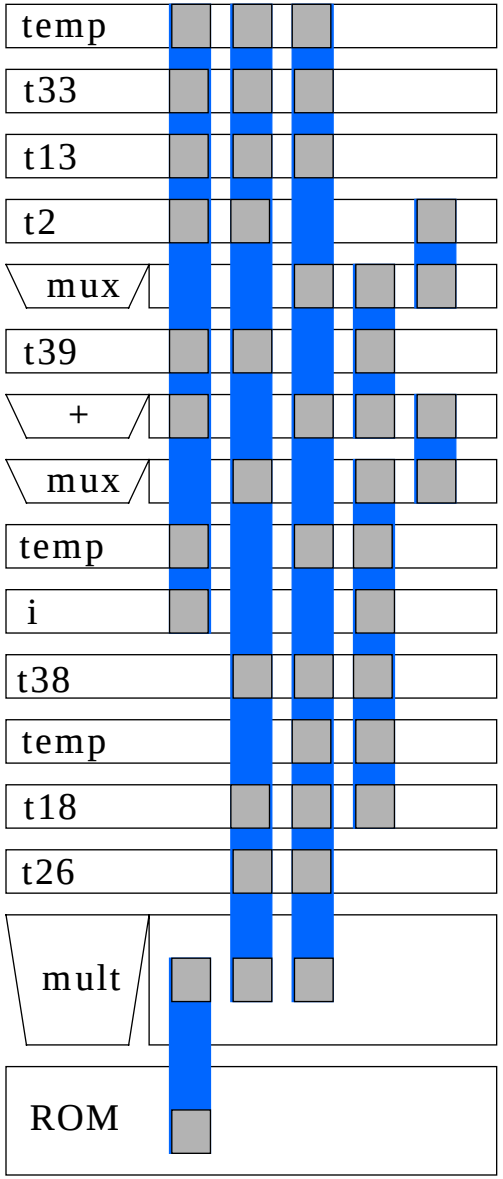
HAL Example

- Sized Cells
- 4 tracks, wirelength = 1577



Elliptic Filter

- 1 multiply, 1 adder (4 clock multiply)
- Sized Cells
- 5 tracks, wirelength 3326 (26cpu sec.)



Chip HDL { while(~b)

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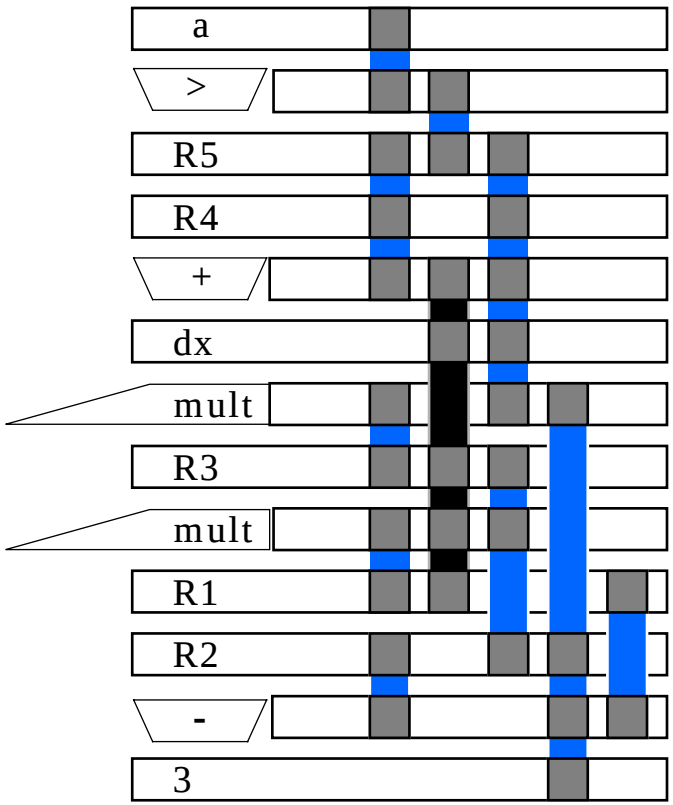
Results

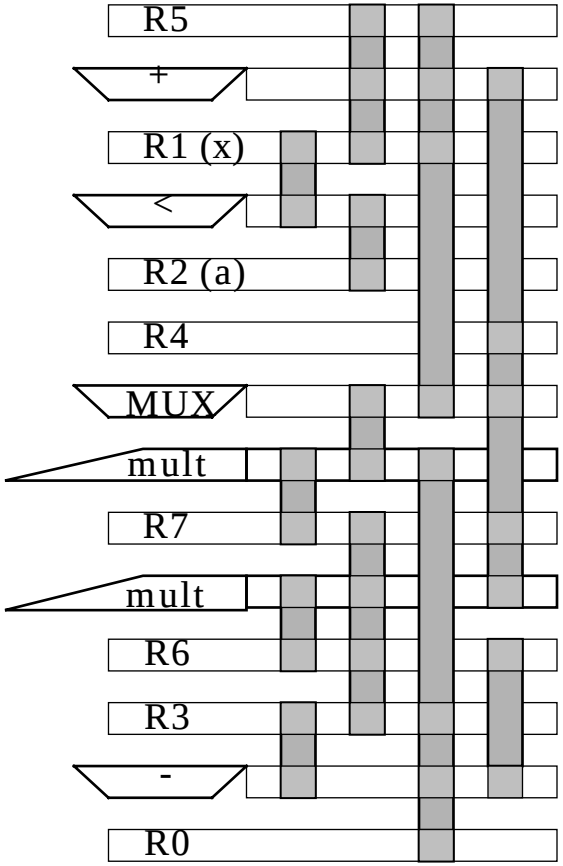
Sample	Tracks	Wirelength	Busses	D.P. Mux	Muxinputs
Hal	4	33	12	1	11
PHal*	5	27	3(7)	1	10
SHal**	5	31	10	3	9
Ellip	5	3326	7	2	26
Hal	4	1577	12	1	11

Example	Tracks	Load Balanced
DE1	4	Yes
DE2	4	Yes
DE3	5	Yes
DE4	4	No
DE5	5	No
DE6	4	No
AFB	6min	Yes
AFU	5min	No

Conclusions

- Number of Busses is Poor Estimate of Number of Tracks
- Use Caution in Minimizing Number of Busses in Scheduler
- Designs with More than Minimal Number of Registers Can Win
- In 1-D Layout, Load Balanced Schedules May Not Be Track Efficient





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