Issues in High-Level Connectivity Synthesis

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Introduction

- Concurrent Interconnection Synthesis and 1-D Layout Generation
- Multiplexer/Bus Trade-Offs
- Busses, Registers, and Tracks

Related Work

- Hercules, ELF, HAL, LYRA, MAHA, Facet
- PARBUS, CATHERAL-II, SPAID, SYCO, BUD
System

VHDL → Compiler → State Graph → Splicer → Design

Functional Units

Placer

Chip HDL { while(~b) }
Model and Constraints For these Experiments

- 1-D Bit-Sliced Placement Model
- Track Minimization Primary Objective
- Sized Cells
- Busses Used Once per Clock Cycle
- Unidirectional Data Transfers
- Cell Inputs are Not Latched
- Minimum Register Designs
## Connectivity to Layout Mapping

<table>
<thead>
<tr>
<th>C1</th>
<th>R1</th>
<th>R2</th>
<th>F1</th>
<th>F2 (Outputs)</th>
<th>Bus1</th>
<th>Bus2</th>
<th>Bus3</th>
<th>Bus4</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
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</tr>
</tbody>
</table>

Inputs: F1, F2a, F2b, R1, R2

- Multiple drives here are bus drivers
- Multiple drives here are multiplexers

Connectivity to Layout Mapping
Busses, Registers, and Tracks

- Number of Tracks Needed In a Design is not Equivalent to Number of Busses

- More Than the Minimal Number of Registers In a Design Can Save Tracks

- What Is The Maximum Number of Tracks Necessary In a Design, If the Number of Registers is not Minimized?

Lemma:

An Upper Bound is Number of Simultaneously Active Functional Unit Outputs Plus 2*binary operations
HAL Example

- Sized Cells
- 4 tracks, wirelength = 1577
Elliptic Filter

- 1 multiply, 1 adder (4 clock multiply)
- Sized Cells
- 5 tracks, wirelength 3326 (26cpu sec.)
## Results

<table>
<thead>
<tr>
<th>Sample</th>
<th>Tracks</th>
<th>Wirelength</th>
<th>Busses</th>
<th>D.P. Mux</th>
<th>Muxinputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hal</td>
<td>4</td>
<td>33</td>
<td>12</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>PHal*</td>
<td>5</td>
<td>27</td>
<td>3(7)</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>SHal**</td>
<td>5</td>
<td>31</td>
<td>10</td>
<td>3</td>
<td>9</td>
</tr>
<tr>
<td>Ellip</td>
<td>5</td>
<td>3326</td>
<td>7</td>
<td>2</td>
<td>26</td>
</tr>
<tr>
<td>Hal</td>
<td>4</td>
<td>1577</td>
<td>12</td>
<td>1</td>
<td>11</td>
</tr>
</tbody>
</table>

### Example

<table>
<thead>
<tr>
<th>Tracks</th>
<th>Load Balanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>DE1</td>
<td>Yes</td>
</tr>
<tr>
<td>DE2</td>
<td>Yes</td>
</tr>
<tr>
<td>DE3</td>
<td>Yes</td>
</tr>
<tr>
<td>DE4</td>
<td>No</td>
</tr>
<tr>
<td>DE5</td>
<td>No</td>
</tr>
<tr>
<td>DE6</td>
<td>No</td>
</tr>
<tr>
<td>AFB</td>
<td>Yes</td>
</tr>
<tr>
<td>AFU</td>
<td>No</td>
</tr>
</tbody>
</table>
Conclusions

- Number of Busses is Poor Estimate of Number of Tracks
- Use Caution in Minimizing Number of Busses in Scheduler
- Designs with More than Minimal Number of Registers Can Win
- In 1-D Layout, Load Balanced Schedules May Not Be Track Efficient
Chip HDL {while(~b)
R5
R4 +
dx
mult R3
R1
R2 -
3

MUX +
R1(x)
< R2(a)
R4
mult R7
mult R6
R3 -
R0